UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING CO. LTD., Petitioner,

v.

ARBOR GLOBAL STRATEGIES LLC, Patent Owner.

> IPR2021-00737 Patent RE42,035 E

Before KARL D. EASTHOM, BARBARA A. BENOIT, and SHARON FENICK, *Administrative Patent Judges*.

EASTHOM, Administrative Patent Judge.

DECISION Granting Institution of *Inter Partes* Review 35 U.S.C. § 314 Granting Motion for Joinder 35 U.S.C. § 315(c); 37 C.F.R. § 42.122

IPR2021-00737 Patent RE42,035 E

On April 5, 2021, Taiwan Semiconductor Manufacturing Co. Ltd. ("Petitioner") filed a Petition (Paper 1, "Pet.") seeking *inter partes* review of claims 1–38 (the "challenged claims") of U.S. Patent No. RE42,035 E (Ex. 1104, "the '035 patent"). With the Petition, Petitioner filed a Motion for Joinder (Paper 3, "Motion" or "Mot.") with *Xilinx, Inc., v. Arbor Global Strategies LLC*, IPR2020-01570 (the "Xilinx '035 IPR"). Subsequently, during a conference call held on May 20, 2021, counsel for Patent Owner, Arbor Global Strategies LLC, confirmed that no opposition to the Motion had been filed and stated that no preliminary response to the Petition will be filed in view of representations that Petitioner made in its Motion. *See* Paper 8 (Order documenting the conference call).

The Board has authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a) (2020). Under 35 U.S.C. § 314(a), an *inter partes* review may not be authorized unless the information in the Petition and the Preliminary Response "shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

For the reasons that follow, we institute an *inter partes* review as to the challenged claims of the '035 patent on all grounds of unpatentability presented. We also grant Petitioner's Motion.

I. BACKGROUND

A. Real Parties-in-Interest

Petitioner identifies Taiwan Semiconductor Manufacturing Co. Ltd. and TSMC North America as real parties-in-interest. Pet. 73. Patent Owner identifies Arbor Global Strategies LLC. Paper 6, 1.

B. Related Proceedings

The parties identify *Arbor Global Strategies LLC v. Samsung Electronics Co., Ltd. et al.*, 2:19-cv-00333-JRG-RSP (E.D. Tex.) and *Arbor Global Strategies LLC v. Xilinx, Inc.,* 1:19-cv-1986-MN (D. Del.) as related proceedings. *See* Pet. 73; Paper 6, 1. In addition to the Xilinx '035 IPR to which Petitioner seeks joinder as a party, Patent Owner identifies two other pending *inter partes* reviews, IPR2020-01020 and IPR2021-00391, as pending challenges to the '035 patent. Paper 6, 1.

Concurrent with the instant Petition, Petitioner filed petitions challenging claims in three related patents, specifically IPR2021-00735 challenging U.S. Patent No. 7,126,214 B2, IPR2021-00736 challenging U.S. Patent No. 7,282,951 B2, and IPR2021-00738 challenging U.S. Patent No. 6,781,226 E.

C. The '035 Patent

The '035 patent describes a stack of integrated circuit (IC) die elements including a field programmable gate array (FPGA) on a die, a memory on a die, and a microprocessor on a die. Ex. 1104, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. *Id.* According to the '035 patent, this arrangement "allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost." *Id.* IPR2021-00737 Patent RE42,035 E Figure 4 follows:

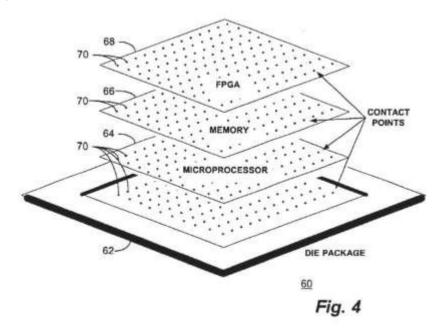


Figure 4 above depicts a stack of dies including FPGA die 68, memory die 66, and microprocessor die 64, interconnected using contact holes 70. Ex. 1104, 4:61–5:4.

The '035 patent explains that an FPGA provides known advantages as part of a "reconfigurable processor." *See* Ex. 1104, 1:17–32. Reconfiguring the FPGA gates alters the "hardware" of the combined "reconfigurable processor" (e.g., the processor and FPGA) making the processor faster than one that simply accesses memory (i.e., "the conventional 'load/store' paradigm") to run applications. *See id.* A "reconfigurable processor" provides a known benefit of flexibly providing the specific functional units required by an application after manufacture. *See id.*

D. Illustrative Claim 1

The Petition challenges independent claims 1, 9, 17, 23, 25, 30, 33, and 36, and dependent claims 2–8, 10–16, 18–22, 24, 26–29, 31, 32, 34, 35, 37, and 38. Claim 1 illustrates the challenged claims at issue:

1. A processor module comprising:

[1.1] at least a first integrated circuit functional element including a programmable array that is programmable as a processing element; and

[1.2] at least a second integrated circuit functional element stacked with and electrically coupled to said programmable array of said first integrated circuit functional element [1.3] wherein said first and second integrated circuit functional elements are electrically coupled by a number of contact points distributed throughout the surfaces of said functional elements and [1.4] wherein said second integrated circuit includes a memory array functional to accelerate external memory references to the processing element.

[1.3] wherein said first and second integrated circuit die elements are electrically coupled by a number of contact points distributed throughout the surfaces of said die elements, and wherein said contact points traverse said die elements through a thickness thereof.

Ex. 1104, 6:11-22 (alterations by Board to conform to Petitioner's

nomenclature).

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