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Paper 34
Date: March 2, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner,

v.

ARBOR GLOBAL STRATEGIES, LLC,
Patent Owner.

IPR2020-01567[1]
Patent 7,126,214 B2

Before KARL D. EASTHOM, BARBARA A. BENOIT, and SHARON FENICK, *Administrative Patent Judges*.

BENOIT, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

[1] Taiwan Semiconductor Manufacturing Co. Ltd. filed a petition in IPR2021-00735 and has been joined as a party to IPR2020-01567.

Xilinx, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1–6 and 26–31 (the "challenged claims") of U.S. Patent No. 7,126,214 B2 (Ex. 1001, "the '214 patent"). Pet. 1. Petitioner filed a Declaration of Paul Franzon, Ph.D. (Ex. 1002) with its Petition. Arbor Global Strategies LLC ("Patent Owner") filed a Preliminary Response (Paper 9, "Prelim. Resp."). We determined that the information presented in the Petition established that there was a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims, and on March 5, 2021, we instituted this proceeding as to all challenged claims and all grounds of unpatentability. Paper 13 ("Institution Decision" or "Inst. Dec.").

After institution, Taiwan Semiconductor Manufacturing Co. Ltd. ("TSM") filed a Petition seeking *inter partes* review of the claims challenged in this proceeding and a Motion for Joinder. IPR2021-00735, Papers 1, 3, 5.[2] We instituted an *inter partes* review in IPR2021-00735 and joined TSM as a party to this proceeding. Paper 20.

Subsequently, Patent Owner filed a Patent Owner Response (Paper 19, "PO Resp.") and a declaration of Shukri Souri, Ph.D. in support thereof (Ex. 2011); Petitioner filed a Reply (Paper 23, "Pet. Reply") and a supplemental declaration of Dr. Franzon in support thereof (Ex. 1070); and Patent Owner filed a Sur-reply (Paper 27, "PO Sur-reply"). Thereafter, the parties presented oral arguments, and the Board entered a transcript into the record. Paper 33 ("Tr.").

[2] The petition in IPR2021-00735 (Paper 1) filed on April 5, 2021 was replaced by a corrected petition (Paper 5), which was accepted by the Board (Paper 7).

We have jurisdiction under 35 U.S.C. § 6(b)(4). For the reasons set forth in this Final Written Decision pursuant to 35 U.S.C. § 318(a), we determine that Petitioner demonstrates by a preponderance of evidence that the challenged claims are unpatentable.

I. BACKGROUND

A. Real Parties-in-Interest

As the real parties-in-interest, Petitioner identifies itself (Pet. 48) and TSM identifies itself and TSMC North America (IPR2021-00735, Paper 5, 48). Patent Owner identifies Arbor Global Strategies LLC. Papers 4, 1; 6, 1.

B. Related Proceedings

The parties identify *Arbor Global Strategies LLC* v. *Xilinx, Inc.,* 1:19-cv-1986-MN (D. Del.) (filed October 18, 2019) as a related proceeding. *See* Pet. 48; Papers 4, 1; 6, 1.

Concurrent with the instant Petition, Petitioner filed petitions challenging claims in three related patents, respectively IPR2020-01568 challenging U.S. Patent No. 7,282,951 ("the '951 patent"), IPR2020-01570 challenging U.S. Patent No. RE42035, and IPR2020-01571 challenging U.S. the 6,781,226 patent. *See, e.g.*, Pet. 48. These three patents also have been challenged by a different petitioner in IPR2020-01020, IPR2020-01021 ("IPR-1021"), and IPR2020-01022. The joined party here (TSM) also was joined as a party to each of those proceedings.

C. The '214 patent

The '214 patent describes a stack of integrated circuit ("IC") die elements including a field programmable gate array (FPGA) on a die, a

memory on a die, and a microprocessor on a die. Ex. 1001, code (57), Fig. 4. Multiple contacts traverse the thickness of the die elements of the stack to connect the gate array, memory, and microprocessor. Ex. 1001, code (57), Fig. 4. According to the '214 patent, this arrangement "allows for a significant acceleration in the sharing of data between the microprocessor and the FPGA element while advantageously increasing final assembly yield and concomitantly reducing final assembly cost." Ex. 1001, code (57), Fig. 4.

Figure 4 follows:

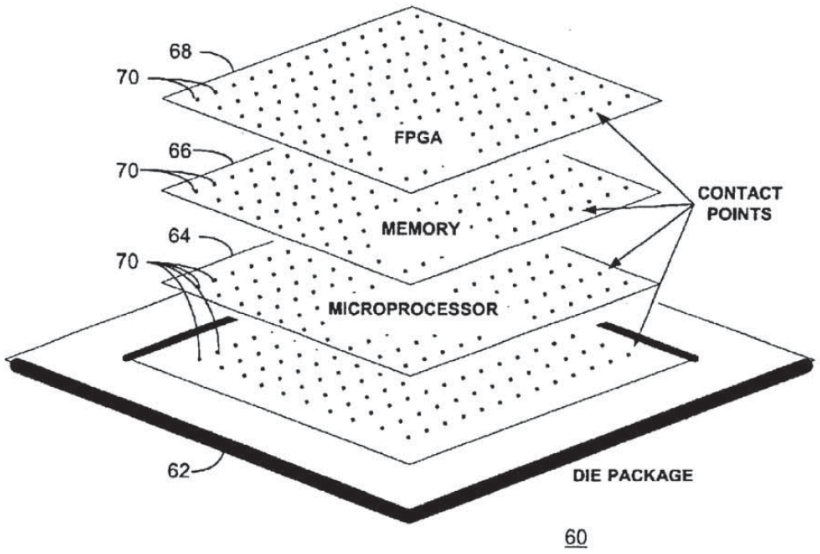

Fig. 4

Figure 4 above depicts a stack of dies including FPGA die 68, memory die 66, and microprocessor die 64, interconnected using contact holes 70. Ex. 1001, 4:59–5:2.

The '214 patent explains that an FPGA provides known advantages as part of a "reconfigurable processor." *See* Ex. 1001, 1:23–39. Reconfiguring the FPGA gates alters the "hardware" of the combined "reconfigurable processor" (e.g., the processor and FPGA) making the processor faster than

one that simply accesses memory (i.e., "the conventional 'load/store' paradigm") to run applications. *See* Ex. 1001, 1:23–39. A "reconfigurable processor" provides a known benefit of flexibly providing the specific functional units needed for applications to be executed. *See* Ex. 1001, 1:23–39.

D. Illustrative Claim

The Petition challenges claims 1–6 and 26–31, of which claims 1, 2, 26, and 27 are independent claims. Each of the challenged claims are directed toward a programmable array module. *See, e.g.,* Ex. 1001, 7:56 (independent claim 1), 8:2 (independent claim 2), 9:41 (independent claim 26), 9:52. Claim 1, reproduced below with bracketed numbering added for reference, illustrates the challenged claims at issue:

> 1. A programmable array module comprising:
>
> [1.1] at least a first integrated circuit functional element including a field programmable gate array; and
>
> [1.2] at least a second integrated circuit functional element including a memory array stacked with and electrically coupled to said field programmable gate array of said first integrated circuit functional element
>
> [1.3] wherein said field programmable gate array is programmable as a processing element, and
>
> [1.4] wherein said memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element.

Ex. 1001, 7:56–67.

Among the differences recited by the independent claims, independent claims 2 and 27 recite "said first and second integrated circuit functional elements being coupled by a number of contact points distributed throughout

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