Micron Technology, Inc. Petitioner v. Vervain, LLC Patent Owner

Case No. IPR2021-01550 U.S. Patent No. 10,950,300

Micron's Hearing Demonstratives

January 12, 2023

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DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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dmap

The 300 Patent

The Remaining Dispute: RAM Cache in Dusija's Controller

The Petition's Showing of RAM Cache in Dusija's Controller

Petitioner's Showing Remains Unrebutted

PO's Arguments Are Without Merit

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DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

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300 Patent

The specification discloses performing a data integrity test" on data stored in MLC NAND flash by:

- retaining in DRAM a copy of data to be written to the flash memory;
- 2. writing the data to the flash memory;
- reading the data back from the flash memory; and
- 4. comparing the data read back from the flash memory *to the data retained in the DRAM*.

f the data integrity test fails, the data is written to the SLC NAND flash memory nodule.

A "read-modify-write" scheme is used to write data to the NAND flash. Data to be written to NAND flash is maintained in DRAM 20. After each write to an address within a particular address range, the device controller 14 will—as time permits—perform a read on the address range to ensure the integrity of the written data. If a data integrity test fails, the address range is remapped from the MIC NAND flash memory module 26 to the next available address range in the SLC NAND flash memory module 28.

Ex. 1007 (300 Patent), 5:59-67.

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

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300 Patent – "Random Access Volatile Memory" in Claim 1

. A system for storing data comprising:

nemory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;

- t least one controller to operate memory elements and associated memory space;
- t least one MLC nonvolatile memory element that can be mapped into the MLC memory space;
- t least one SLC nonvolatile memory element that can be mapped into the SLC memory space;

t least one random access volatile memory;

n FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory;

ne controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;

- the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory;
- wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and
- wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

Ex. 1007 (300 Patent), Claim 1.

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