



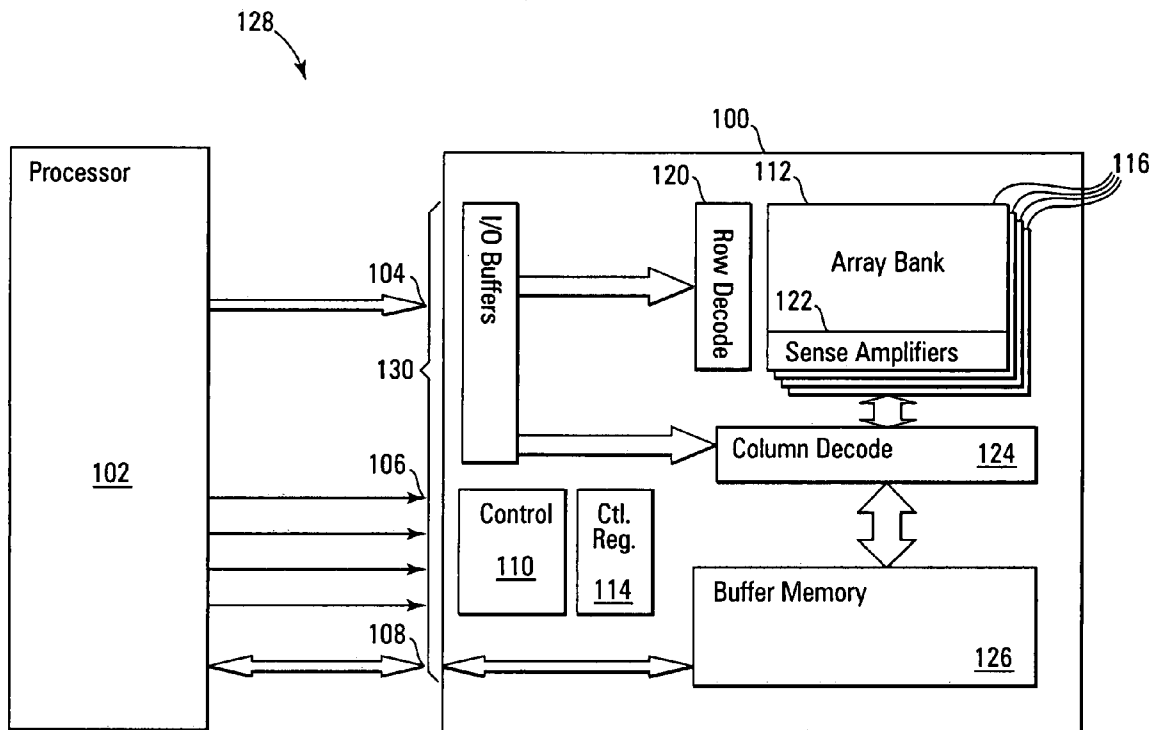
US 20050204091A1

(19) **United States**(12) **Patent Application Publication****Kilbuck et al.**(10) **Pub. No.: US 2005/0204091 A1**(43) **Pub. Date: Sep. 15, 2005**(54) **NON-VOLATILE MEMORY WITH
SYNCHRONOUS DRAM INTERFACE**(57) **ABSTRACT**(76) Inventors: **Kevin M. Kilbuck**, Boise, ID (US);
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LEFFERT JAY & POLGLAZE, P.A.**P.O. BOX 581009****MINNEAPOLIS, MN 55458-1009 (US)**(21) Appl. No.: **10/798,795**(22) Filed: **Mar. 11, 2004****Publication Classification**(51) **Int. Cl.⁷ G06F 12/00**(52) **U.S. Cl. 711/103**

A high density non-volatile memory system, card, and device is described that incorporates a synchronous interface. This is accomplished through use of an external or embedded controller and/or memory buffer to manage the high density non-volatile memory device(s) to present it as a conventional memory device having a synchronous interface that is accessible by row and column address. This allows the high density non-volatile memory to support in-place code execution and allows it to be booted from. Additionally, this incorporation eliminates the overhead of drivers and/or operating system support required to utilize and present conventional high density non-volatile memory devices and moves it internal to the memory device. This simplifies the use and design effort in the overhead and specialized interfacing of high density non-volatile memories and in particular, NAND architecture Flash memories, while reducing the production cost through use of less expensive high density non-volatile memory.



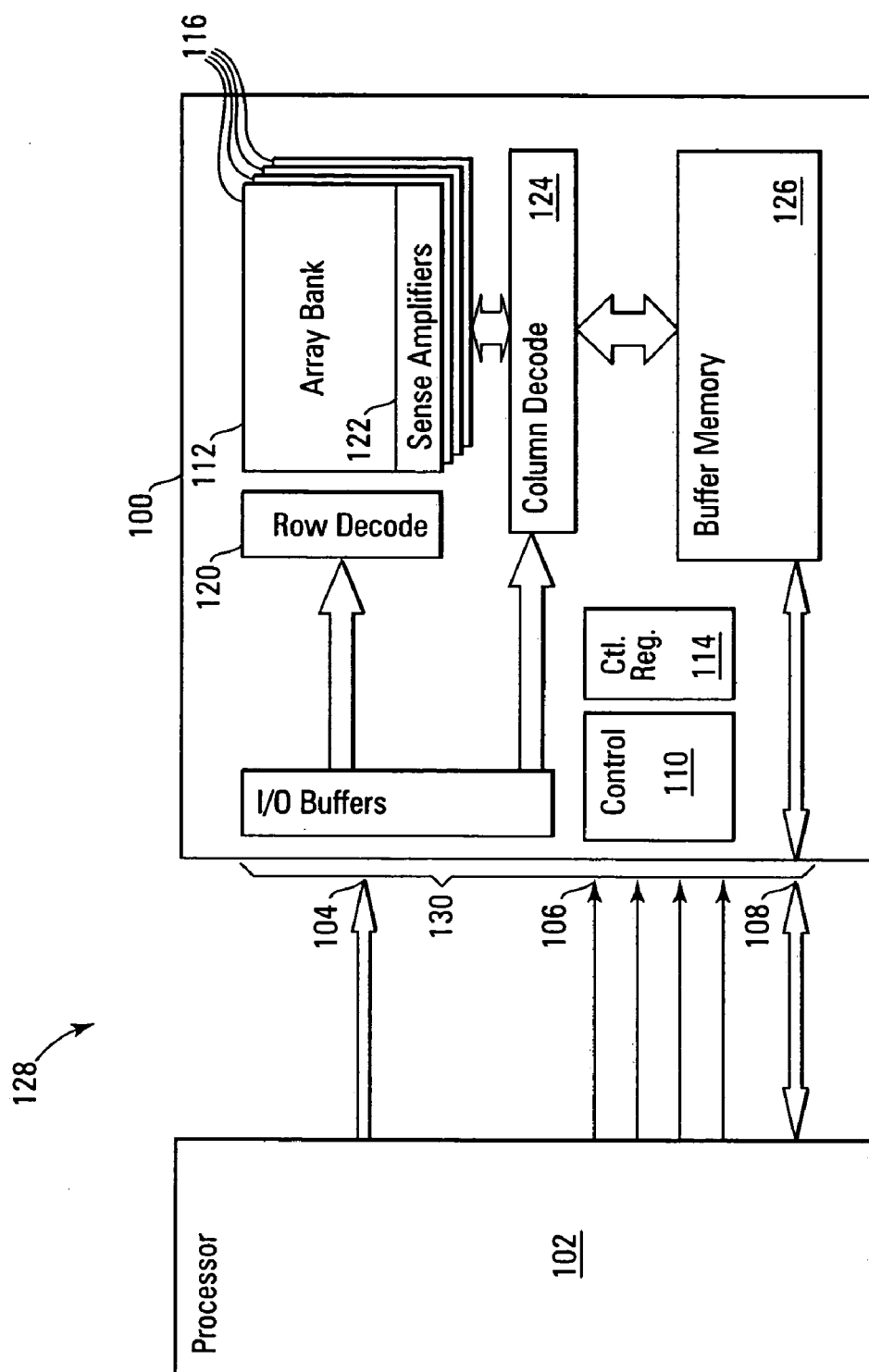
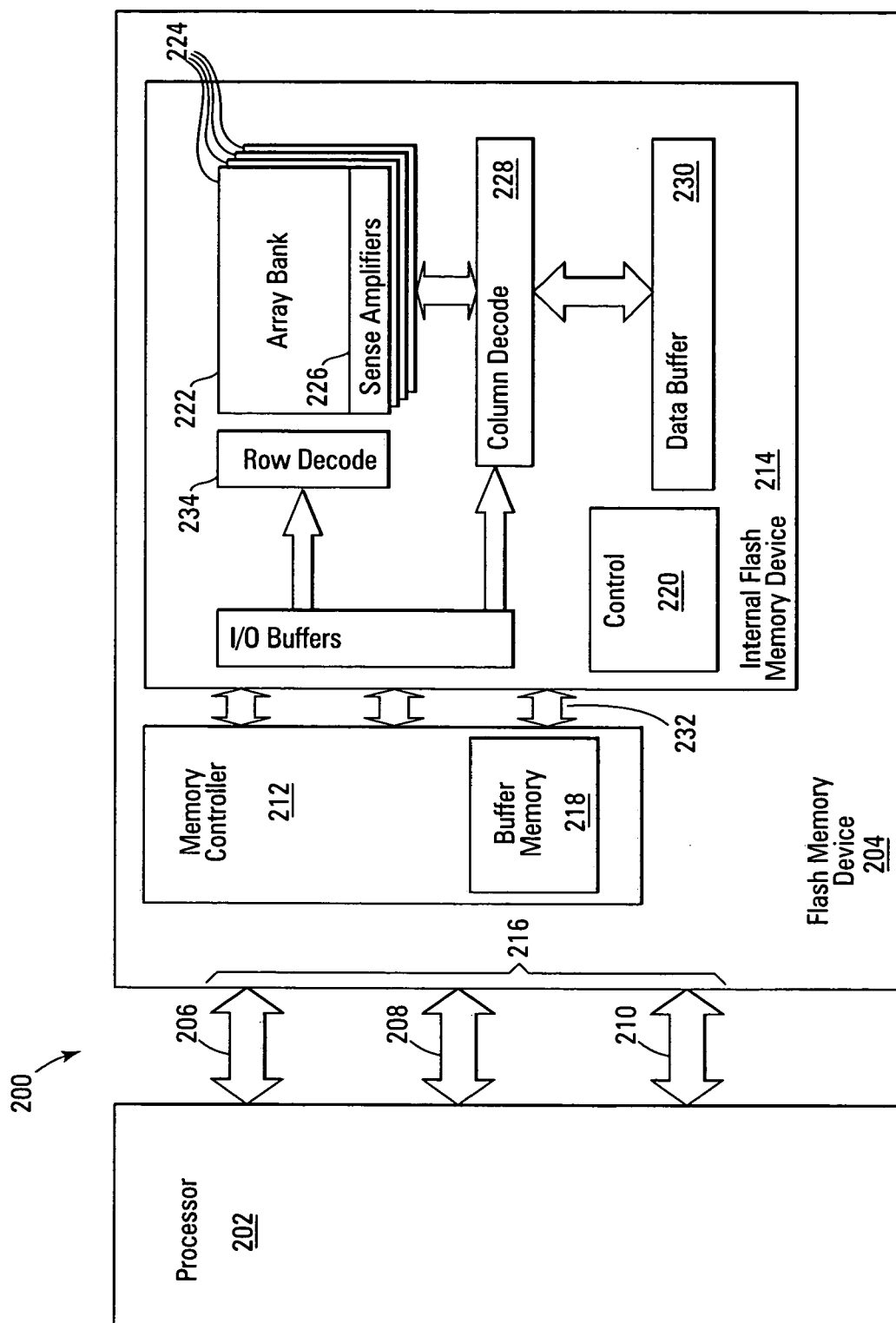


Fig. 1



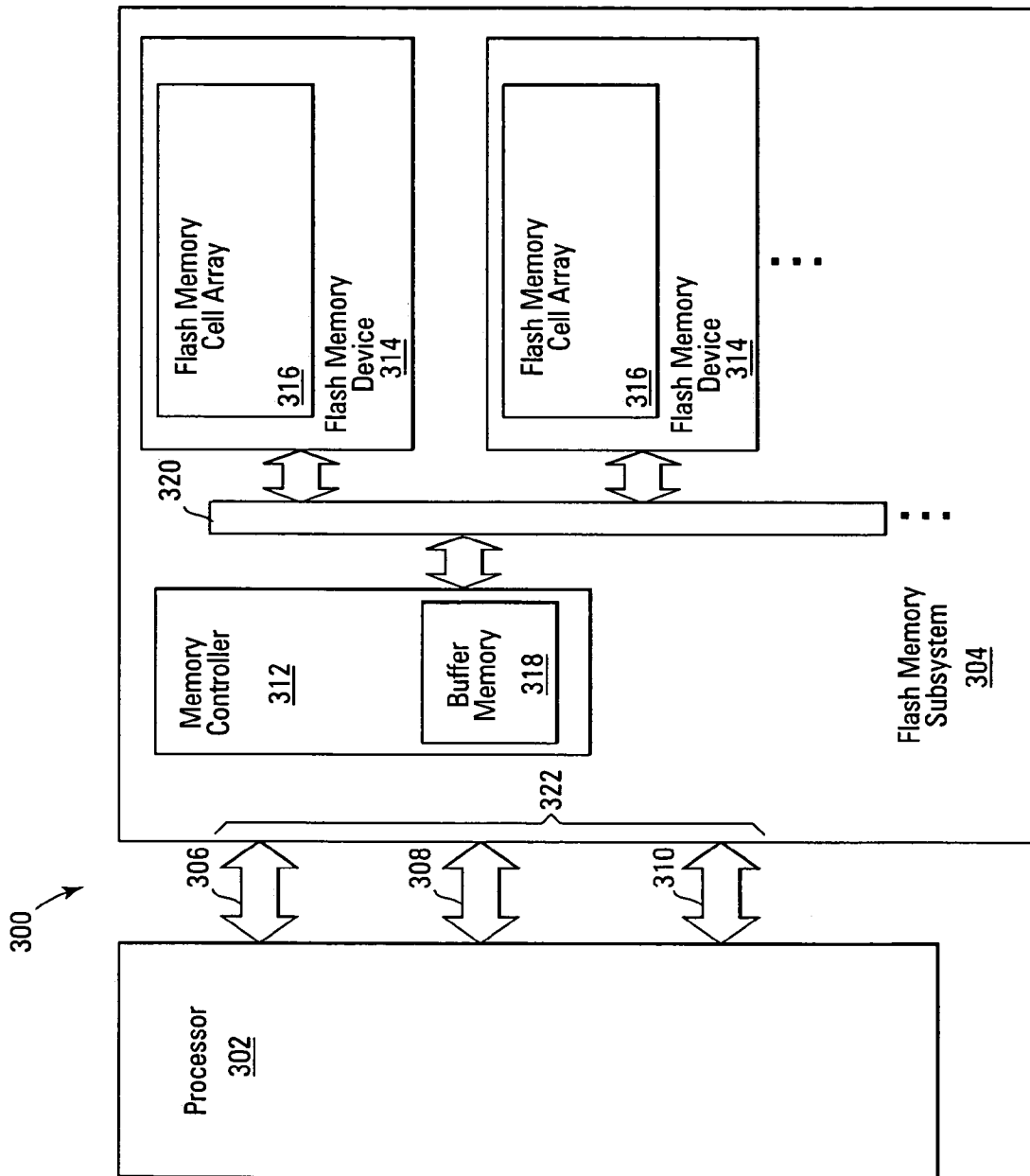


Fig. 3A

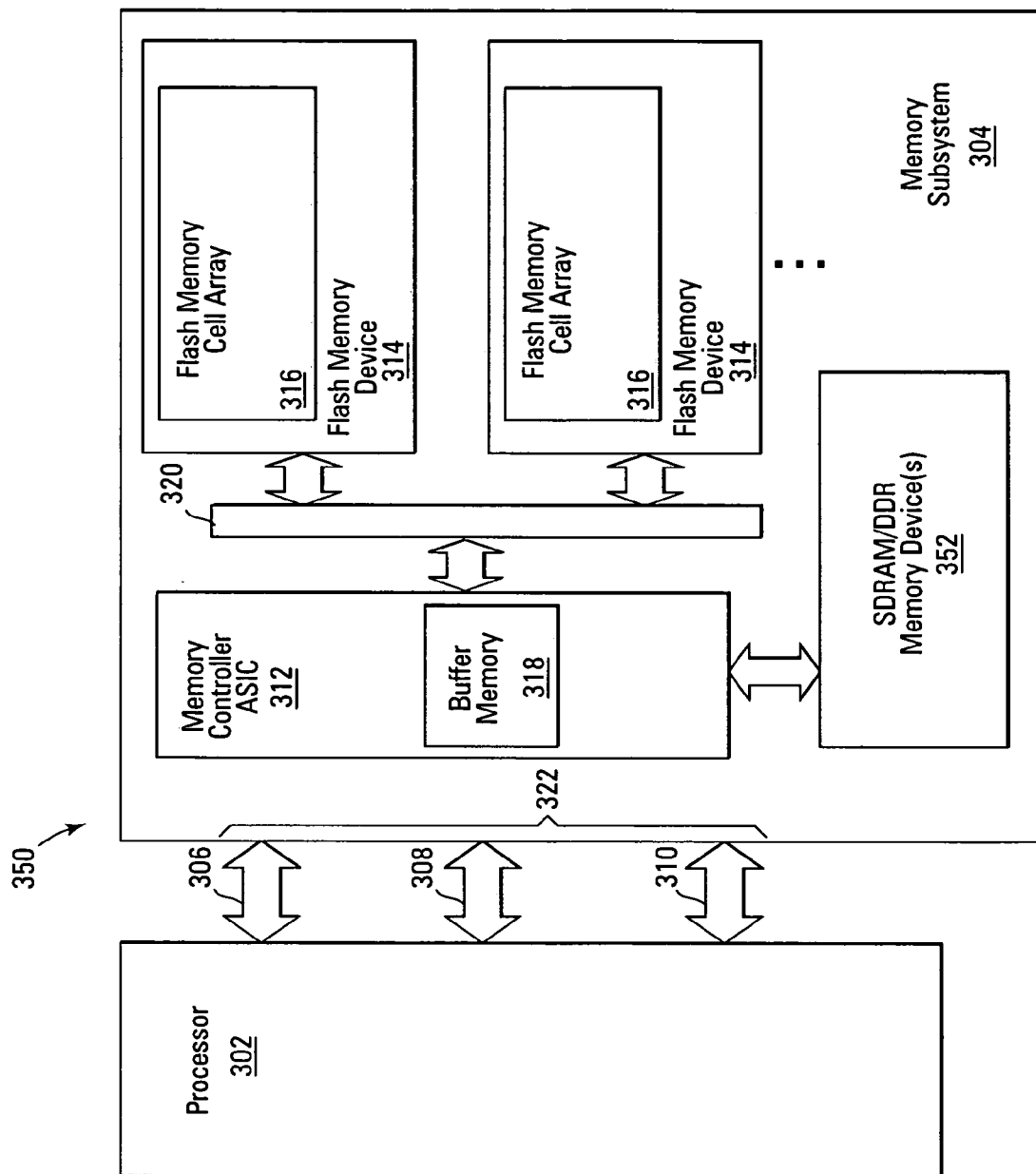


Fig. 3B



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