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**Okuno et al.**

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(54) **STORAGE CONTROLLER AND CONTROL METHOD THEREOF**

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(73) Assignee: **Hitachi, Ltd.**, Tokyo (JP)

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(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 514 days.

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(21) Appl. No.: **11/698,022**

(57) **ABSTRACT**

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**  
**G06F 13/10** (2006.01)

(52) **U.S. Cl.** ..... 711/113; 711/114; 711/E12.025;  
711/E12.035; 714/6; 714/9; 714/E11.092;  
710/22

(58) **Field of Classification Search** ..... 711/100,  
711/112

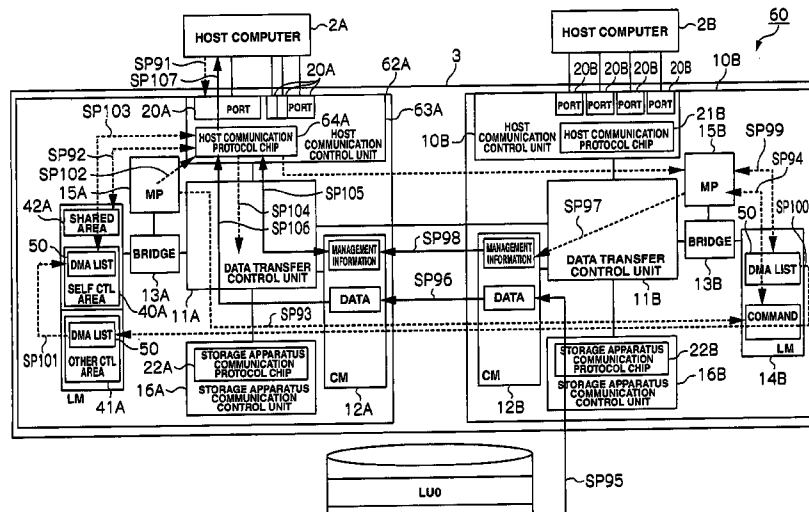
See application file for complete search history.

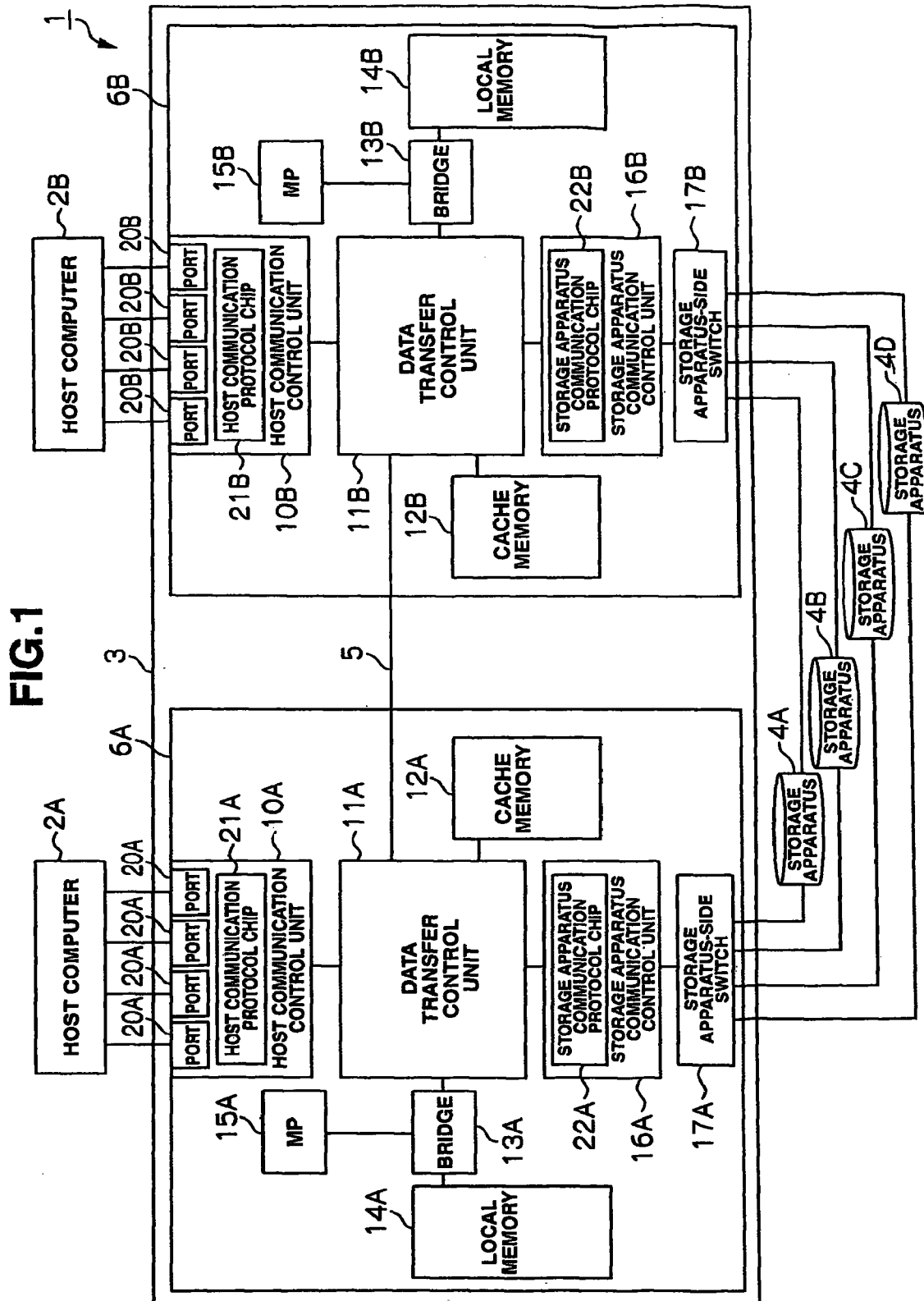
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**12 Claims, 18 Drawing Sheets**





**FIG. 2A****■ MEMORY SPACE VIEWED FROM PROCESSOR**

ARD	CTL0 MEMORY MAP (CTL0 PROCESSOR SIDE)	CTL1 MEMORY MAP (CTL1 PROCESSOR SIDE)
0x0_00000000-0x0_7FFFFFFF	CT_0 LOCAL MEMORY	CTL1 LOCAL MEMORY
0x0_80000000-0x0_FFFFFFFF	CT_0 BRIDGE REGISTER	CTL1 BRIDGE REGISTER
0x1_00000000-0x1_7FFFFFFF	CT_0 HOST COMMUNICATION PROTOCOL CHIP REGISTER	CTL1 HOST COMMUNICATION PROTOCOL CHIP REGISTER
	CT_0 STORAGE APPARATUS COMMUNICATION PROTOCOL CHIP REGISTER	CTL1 STORAGE APPARATUS COMMUNICATION PROTOCOL CHIP REGISTER
0x1_80000000-0x1_FFFFFFFF	CT_0 DATA TRANSFER CONTROL UNIT REGISTER	CTL1 DATA TRANSFER CONTROL UNIT REGISTER
0x2_00000000-0x5_FFFFFFFF	CT_0&1 CACHE MEMORY (INCLUDING EXPANSION (1) TO (3))	CTL0&1 CACHE MEMORY (INCLUDING EXPANSION (1) TO (3))
0x6_00000000-0x6_FFFFFFFF	CT_1 LOCAL MEMORY	CTL0 LOCAL MEMORY
0x6_80000000-0x6_FFFFFFFF	CT_1 BRIDGE REGISTER	CTL0 BRIDGE REGISTER
0x7_00000000-0x7_7FFFFFFF	CT_1 HOST COMMUNICATION PROTOCOL CHIP REGISTER	CTL0 HOST COMMUNICATION PROTOCOL CHIP REGISTER
	CT_1 STORAGE APPARATUS COMMUNICATION PROTOCOL CHIP REGISTER	CTL0 STORAGE APPARATUS COMMUNICATION PROTOCOL CHIP REGISTER
0x7_80000000-0x7_7FFFFFFF	CT_1 DATA TRANSFER CONTROL UNIT REGISTER	CTL0 DATA TRANSFER CONTROL UNIT REGISTER
30A		30C
30B		

**FIG. 2B****■ MEMORY SPACE VIEWED FROM HOST COMMUNICATION PROTOCOL CHIP**

ARD	CTL0 MEMORY MAP (CTL0 HOST COMMUNICATION PROTOCOL CHIP SIDE)	CTL1 MEMORY MAP (CTL1 HOST COMMUNICATION PROTOCOL CHIP SIDE)
0x0_00000000-0x0_7FFFFFFF	CT_0 LOCAL MEMORY	CTL1 LOCAL MEMORY
0x0_80000000-0x0_FFFFFFFF	CT_1 LOCAL MEMORY	CTL0 LOCAL MEMORY
0x1_00000000-0xF_7FFFFFFF	CT_0&1 CACHE MEMORY (INCLUDING EXPANSION (1) TO (3))	CTL0&1 CACHE MEMORY (INCLUDING EXPANSION (1) TO (3))
31A	31B	31C

FIG.3A

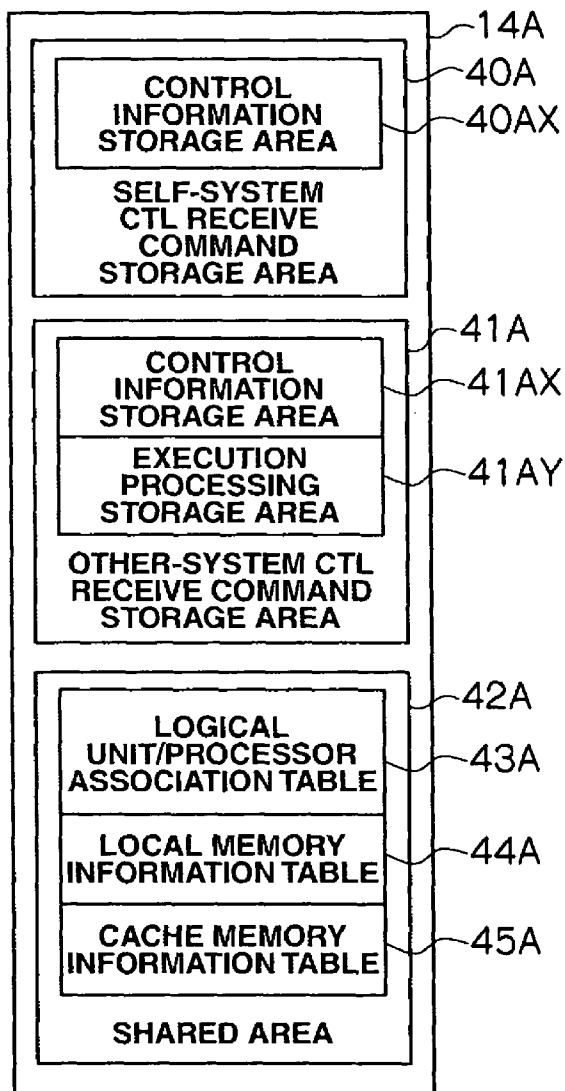


FIG.3B

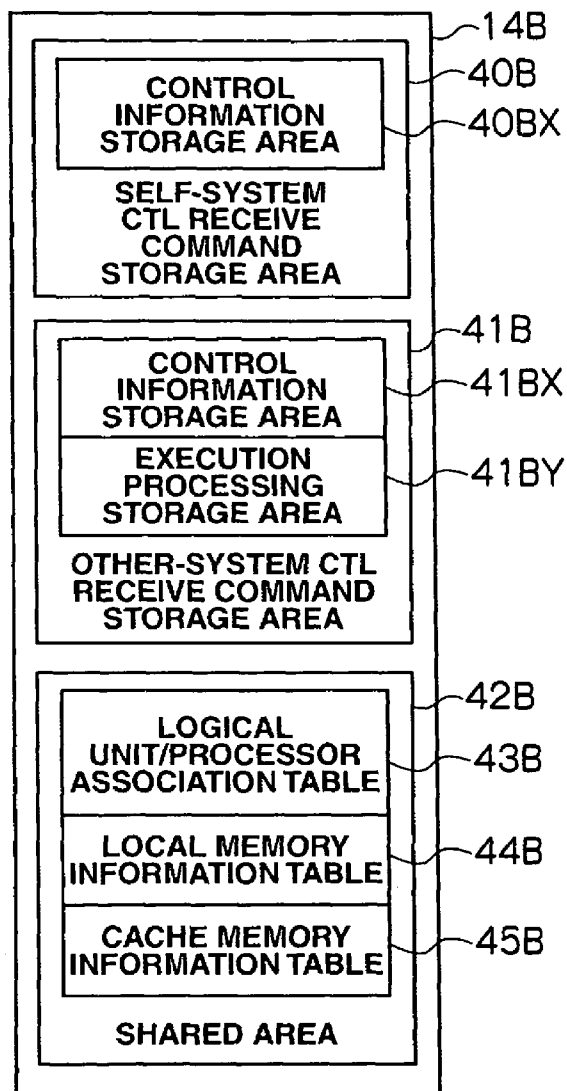


FIG. 4A

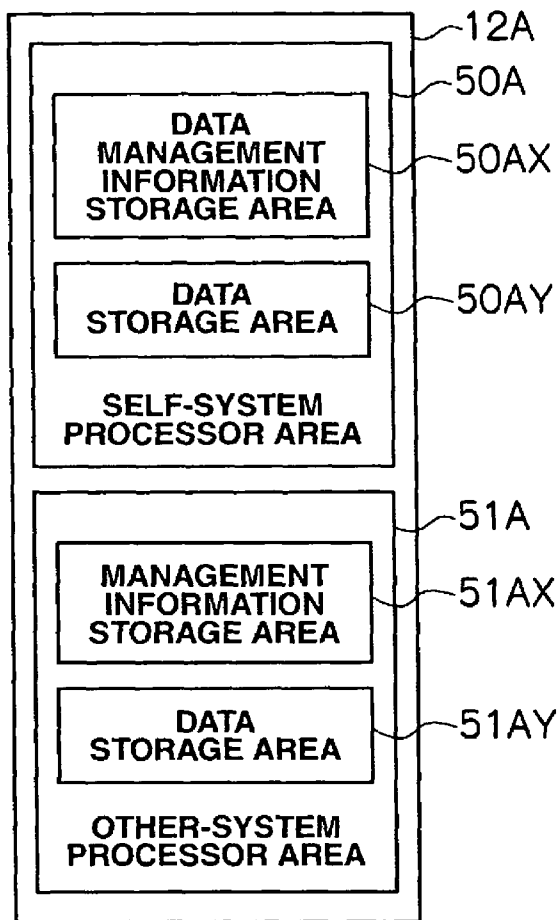
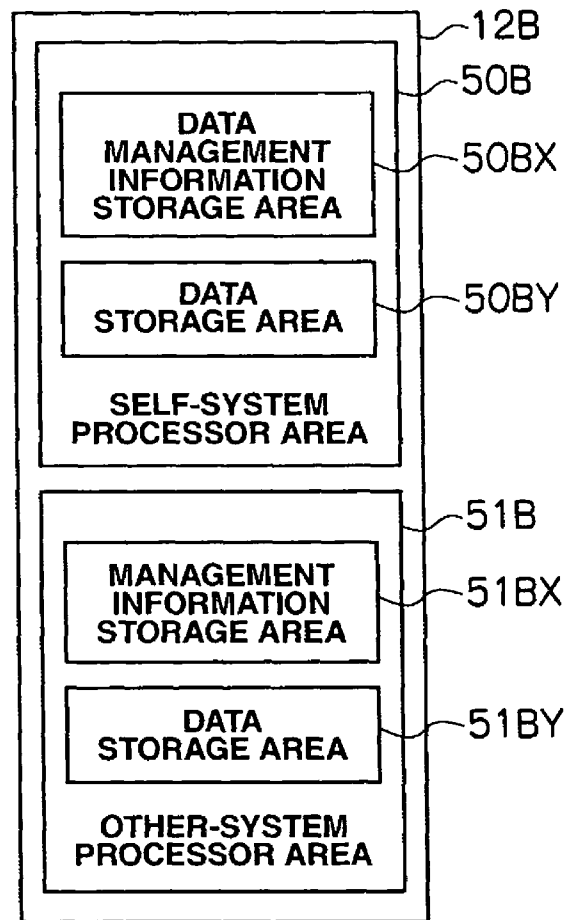


FIG. 4B



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