UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; and MICRON TECHNOLOGY TEXAS LLC, Petitioner,

v.

NETLIST, INC., Patent Owner.

IPR2022-00418 Patent 8,301,833 B1

Before GEORGIANNA W. BRADEN, SHEILA F. McSHANE, and KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

SZPONDOWSKI, Administrative Patent Judge.

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JUDGMENT Final Written Decision Determining All Challenged Claims Unpatentable 35 U.S.C. § 318(a)

I. INTRODUCTION

We instituted *inter partes* review of claims 1, 3–17, and 19–30 of U.S. Patent 8,301,833 B1, issued on October 30, 2012 (Ex. 1001, "the '833 patent") in response to a Petition (Paper 2, "Pet.") filed by Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively "Petitioner"). Paper 14 ("Inst. Dec."). During the trial, Netlist, Inc. ("Patent Owner") filed a Response to the Petition (Paper 19, "PO Resp."), Petitioner filed a Reply (Paper 22, "Reply"), and Patent Owner filed a Sur-reply (Paper 23, "Sur-reply").

An oral hearing was held on June 7, 2023, and a copy of the transcript was entered into the record. Paper 29 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the claims on which we instituted trial. Based on the complete record, Petitioner has shown by a preponderance of the evidence that claims 1, 3–17, and 19– 30 of the '833 patent are unpatentable.

II. BACKGROUND

A. Real Parties-in-Interest

Petitioner identifies itself as the real party-in-interest. Pet. 64. Patent Owner also identifies itself as the real party-in-interest. Paper 3 ("Patent Owner's Mandatory Disclosure"), 1.

B. Related Matters

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The parties advise that the '833 patent is the subject of *Netlist, Inc. v. Micron Technology, Inc., et al.*, 6:21-cv-00430 (W.D. Tex.). Pet. 64; Paper 3, 2. Petitioner also advises that the '833 patent has been the subject of the following three *inter partes* review proceedings: IPR2014-00994,

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IPR2014-01370, and IPR2017-00649. Pet. 64. Additionally, Petitioner advises that "a nearly identical claim to the '833 Patent's claim 15 was invalidated as obvious in IPR2017-00692." *Id.* at 65.

C. The '833 Patent (Ex. 1001)

The '833 patent is titled "Non-Volatile Memory Module" and is generally directed to "a memory system which can communicate with a host system such as a disk controller of a computer system." Ex. 1001, codes (54), (57).

The '833 patent states that "[n]on-volatile memory can generally maintain stored information while power is not applied to the non-volatile memory," so, "[i]n certain circumstances, it can therefore be useful to backup volatile memory using non-volatile memory." *Id.* at 1:28–31. The invention in the '833 patent relates to a configuration of hybrid memory systems that "can include volatile and non-volatile memory and a controller which are configured such that the controller backs up the volatile memory using the non-volatile memory in the event of a trigger condition," such as a power failure or power reduction. *Id.* at code (57), 3:65–67, 17:66–18:1. "[T]he volatile memory system can be operated at a reduced frequency during backup and/or restore operations which can improve the efficiency of the system and save power." *Id.* at 4:41–44.

Figure 9, which depicts a flowchart of an example method of a volatile memory subsystem operating at a reduced rate in back-up mode, is reproduced below:

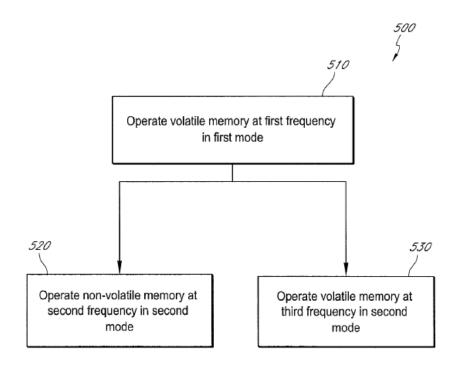


FIG. 9

Id. at 3:45–48. Figure 9 depicts block 510, "[o]perate volatile memory at first frequency in first mode," block 520, "[o]perate non-volatile memory at second frequency in second mode," and block 530, "[o]perate volatile memory at third frequency in second mode." The memory system "may switch from the first mode of operation to the second mode of operation in response to a trigger condition," such as "a power failure condition." *Id.* at 17:64–18:1. The second mode of operation may include, for example, backup and/or restore operations. *Id.* at 18:1–7. The '833 patent also describes that "[t]he third frequency can be less than the first frequency," and "can be approximately equal to the second frequency." *Id.* at 18:8–10.

D. Illustrative Claims

Among the challenged claims, claims 1 and 15 are independent.

Independent claim 15 is representative and is reproduced below.

15. A memory system operatively coupled to a host system, the memory system comprising:

a volatile memory subsystem operable at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;

and a non-volatile memory subsystem operable at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem,

the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

Ex. 1001, 21:61–22:11.

E. Prior Art and Asserted Challenge to Patentability

Petitioner asserts that claims 1, 3–17, and 19–30 are unpatentable on the following challenge (Pet. 2):¹

¹ Petitioner also asserts, as a separate challenge, that Patent Owner is collaterally estopped from re-litigating the issue of validity of claims 1 and 15 of the '833 patent based upon the Final Written Decision in IPR2017-00692, where claim 15 of U.S. Patent No. 8,874,831, which is a continuation-in-part of the '833 patent, was determined invalid over the combination of Best, Bonella, and Mills. Pet. 18–24; IPR2017-00692, Paper 25 at 31–40. Petitioner asserts that claim 15 of the '831 patent is substantively identical to claims 1 and 15 of the '833 patent. Pet. 18. As we

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