

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICROSOFT CORPORATION,  
Petitioner,

v.

THROUGHPUTER, INC.,  
Patent Owner.

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IPR2022-00758  
Patent 10,430,242 B2

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Before MICHAEL R. ZECHER, JOHN A. HUDALLA, and  
MATTHEW S. MEYERS, *Administrative Patent Judges*.

MEYERS, *Administrative Patent Judge*.

DECISION  
Denying Institution of *Inter Partes* Review  
*35 U.S.C. § 314*

## I. INTRODUCTION

### A. *Background and Summary*

Microsoft Corporation (“Petitioner”) filed a Petition requesting to institute an *inter partes* review of claims 1–23 (the “challenged claims”) of U.S. Patent 10,430,242 B2 (Ex. 1001, the “’242 patent”). Paper 2 (“Petition” or “Pet.”). ThroughPuter, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 8 (“Preliminary Response” or “Prelim. Resp.”). With our authorization, Petitioner filed a Reply (Paper 10) and Patent Owner filed a Sur-reply (Paper 11), each of which were limited to addressing whether we have authority to adjudicate the priority issue raised in the Petition and whether we should exercise our discretion to deny the Petition under 35 U.S.C. § 325(d).

An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). Having considered the arguments and evidence presented by Petitioner and Patent Owner, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing on at least one of the challenged claims of the ’242 patent. Accordingly, we do not institute an *inter partes* review of the challenged claims.

### B. *Real Parties in Interest*

The parties identify themselves as the real parties in interest. Pet. 78; Paper 4, 2.

### *C. Related Proceedings*

The parties identify, as matters involving or related to the '242 patent, *ThroughPuter, Inc. v. Microsoft Corporation*, No. 2:22-cv-00344-BJR (W.D. Wash.), which was transferred from the U.S. District Court for the Eastern District of Virginia. Pet. 78; Paper 4, 2. Patent Owner indicates that, “[a]s of August 18, 2022, the related district court litigation has been stayed pending resolution of the present *inter partes* review proceeding.” Paper 9, 2.

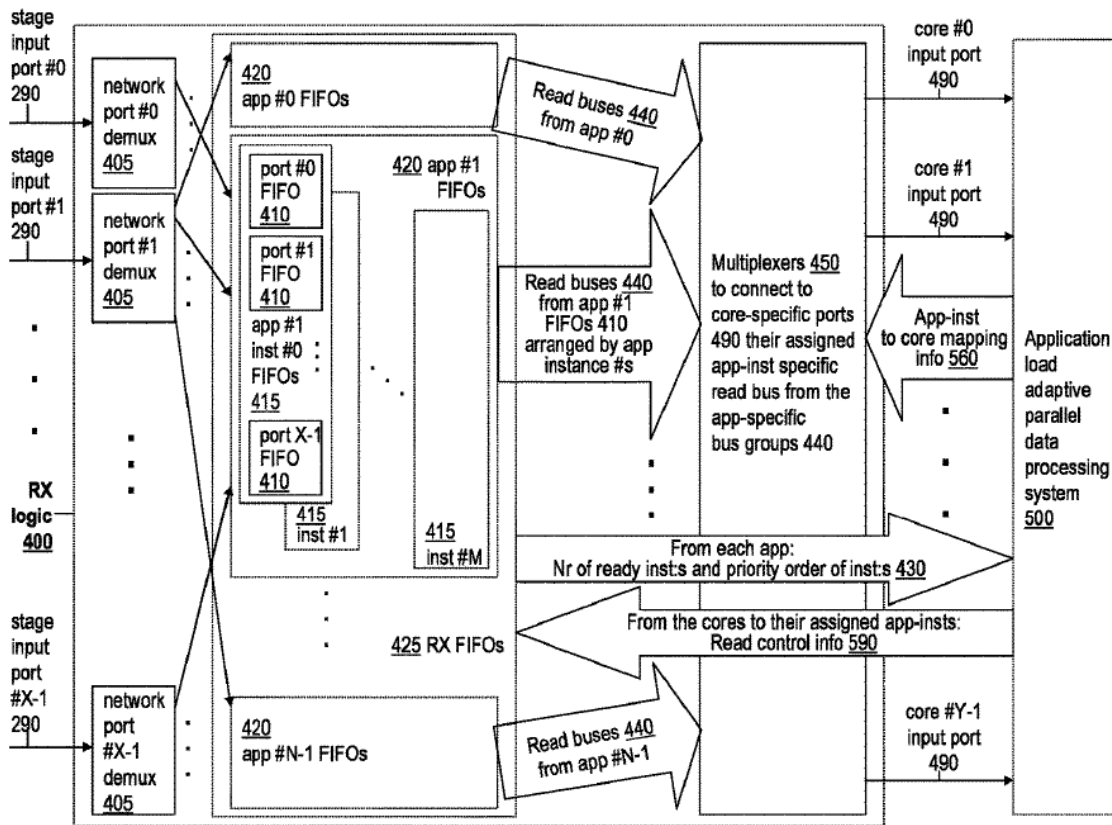
We also note that Petitioner has challenged other patents owned by Patent Owner in IPR2022-00527, IPR2022-00528, IPR2022-00574, and IPR2022-00757.

### *D. The '242 Patent*

The '242 patent is titled “Task Switching and Inter-Task Communications for Coordination of Applications Executing on a Multi-User Parallel Processing Architecture.” Ex. 1001, code (54). The '242 patent describes “an extensible, multi-stage, application program load adaptive, parallel data processing architecture shared dynamically among a set of application software programs according to processing load variations of said programs.” *Id.* at 3:14–18. In particular, a processor with an array of processing cores hosts instances of programs where the array of cores may be allocated among the programs “in part based on volumes of input data packets at the input port buffers associated with individual programs,” and, based in part on this allocation, assigned “for executing specific instances of the programs.” *Id.* at 5:4–24.

In the embodiment shown in Figure 4, reproduced below, the '242 patent describes connecting input packets to processing cores “according to

at which core the destination app-task instance indicated for any given input may be executing at any given time.” *Id.* at 12:34–40.



**FIG. 4**

Figure 4 shows RX (receive) logic subsystem 400 “connecting the input packets from the input ports 290 to the local processing cores” in “manycore processor 500.” *Id.* at 12:42–43. In operation, “input packets arriving over the network input ports 290 are grouped to a set of destination application specific FIFO [first in first out] modules 420, whose fill levels (in part) drives the allocation and assignment of cores at the local manycore processor 500 among instances of the app-tasks hosted on that processor.” *Id.* at 12:57–62. From application-instance specific buffers 415 within FIFO

modules 420, the input packets are connected through multiplexers 450 to specific cores in processor 500, where associated application-instances are executing at a given time. *Id.* at 12:65–13:2.

The '242 patent claims priority to the '473 application through a chain of applications (the “2012 line”), which extends back to several provisional applications, the earliest of which was filed on June 8, 2012. *See id.* at code (60). In addition, the '242 patent claims priority to a provisional application filed on November 4, 2011 through a different chain of applications (the “2011 line”) that does not include the '473 application. *See id.*

#### *E. Illustrative Claim*

Petitioner challenges claims 1–23 of the '242 patent. Pet. 1. Claims 1, 7, and 15 are independent. Claim 1, reproduced below, is representative.

1. A system for managing execution of a plurality of software applications on an array of processing units, the system comprising:

a core fabric comprising

the array of processing units, and

a plurality of input data buffers, each input data buffer being provided for buffering input data directed to a respective software application of the plurality of software applications and being dedicated to the respective software application, wherein

each buffer of the plurality of input data buffers is deployed in the core fabric apart from the array of processing units, and

each software application of the plurality of software applications is provided one or more input data buffers of the plurality of input data buffers; and

a controller comprising hardware logic and/or software logic for performing operations for repeatedly reconfiguring task assignment to the array of processing units, the

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