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United States Patent [19]

Iketani et al.

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[45] Date of Patent: Dec. 30, 1997

[54] **POWER ON RESET CIRCUIT FOR GENERATING RESET SIGNAL AT POWER ON**

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[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo, Japan

[21] Appl. No.: **608,075**

[22] Filed: **Feb. 28, 1996**

[51] **Int. Cl.**[6] **H03L 7/00**

[52] **U.S. Cl.** **327/143**; 327/198; 327/546

[58] **Field of Search** 327/142, 143, 327/198, 399, 544, 545, 546

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Assistant Examiner—Jung Ho Kim
Attorney, Agent, or Firm—Lowe, Price, LeBlanc & Becker

[57] **ABSTRACT**

A power on reset circuit includes a transistor connected between a power supply node and a first node, a first capacitor connected between a ground node and a first node, a resistance element connected parallel to the first capacitor, a first CMOS inverter circuit having an input node connected to the first node and an output node connected to the second node, and a second CMOS inverter circuit having an input node connected to the second node and an output node connected to the first node. Preferably, the power on reset circuit further includes a second capacitor connected between the power supply node and the second node. In the power on reset circuit, when the power is turned off, the first capacitor is fully discharged by the resistance element. Therefore, a reset signal for initializing internal circuitry can be surely generated even when the power is again turned on.

4 Claims, 6 Drawing Sheets

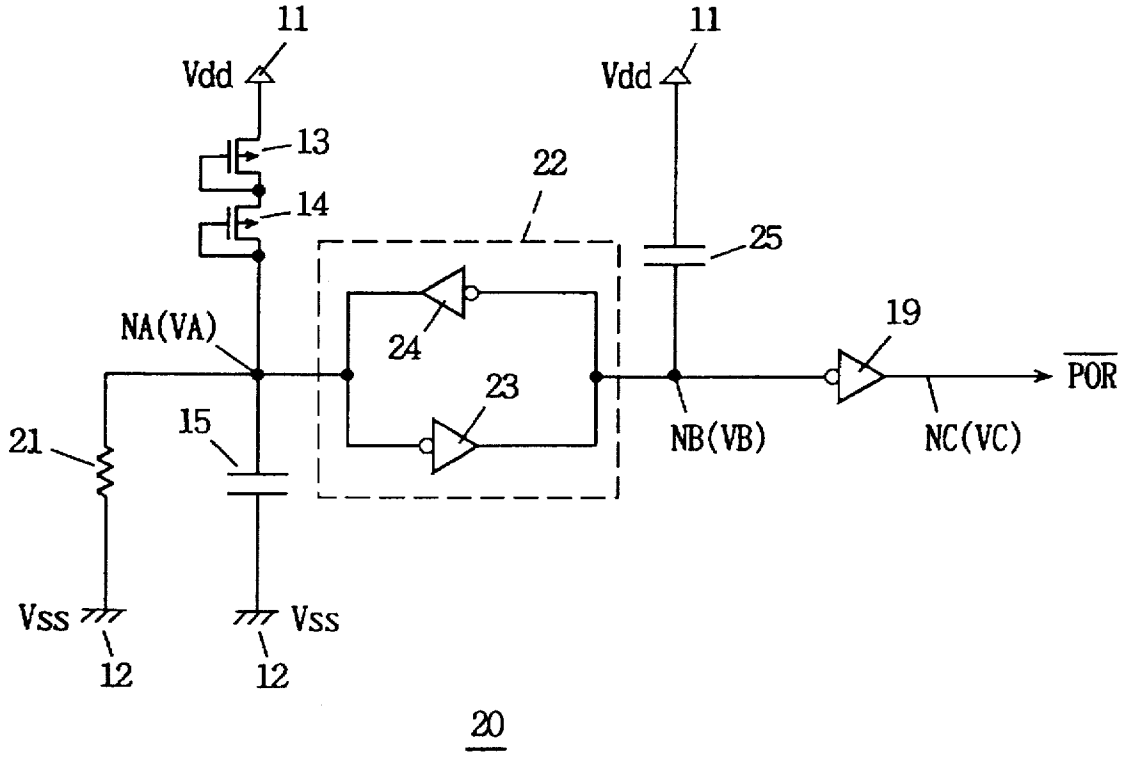

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FIG. 1 PRIOR ART

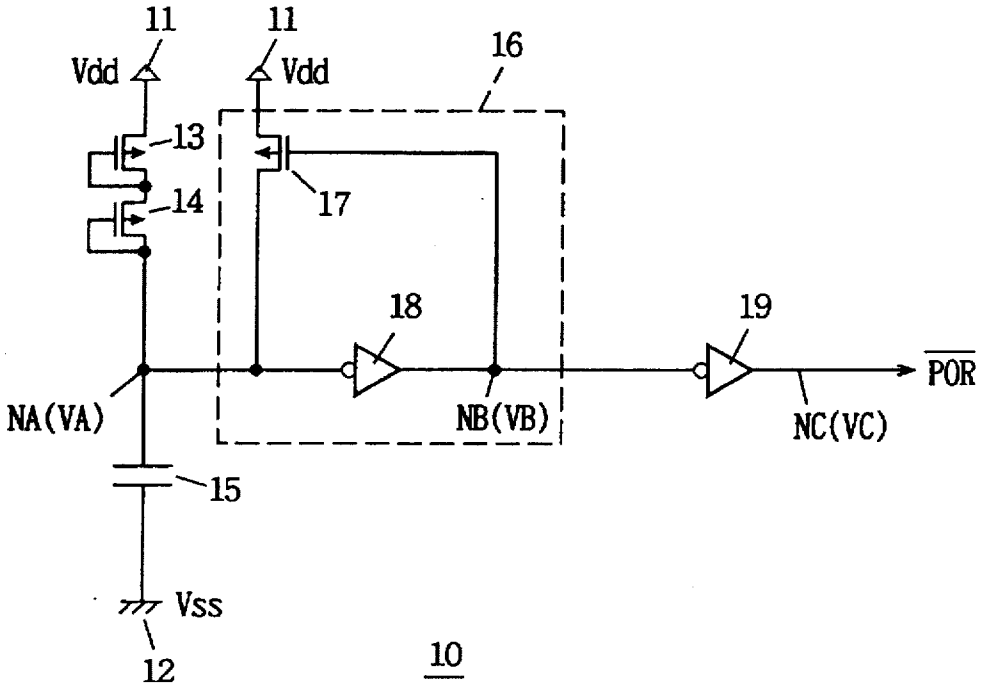

FIG. 2

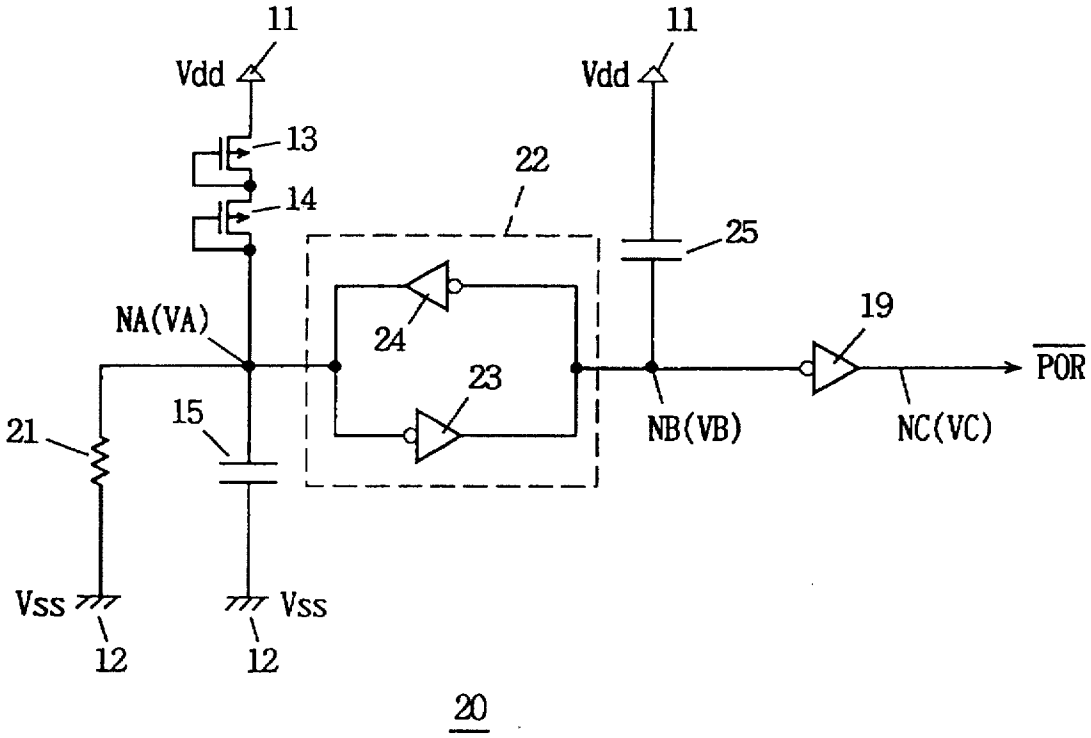

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FIG. 3

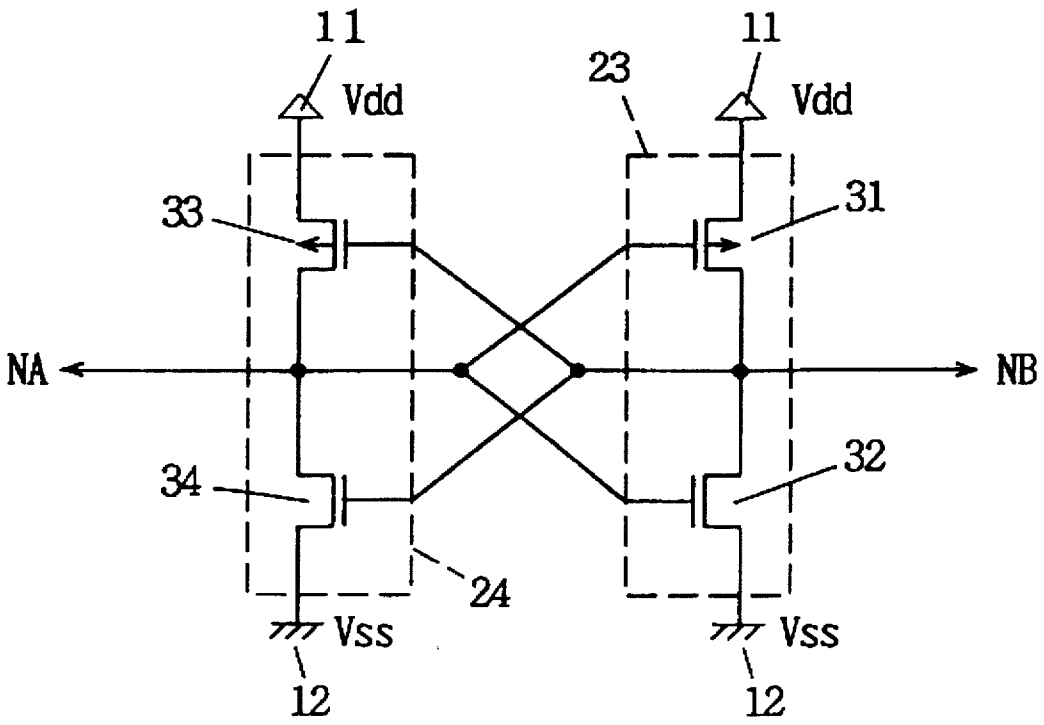

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FIG. 4

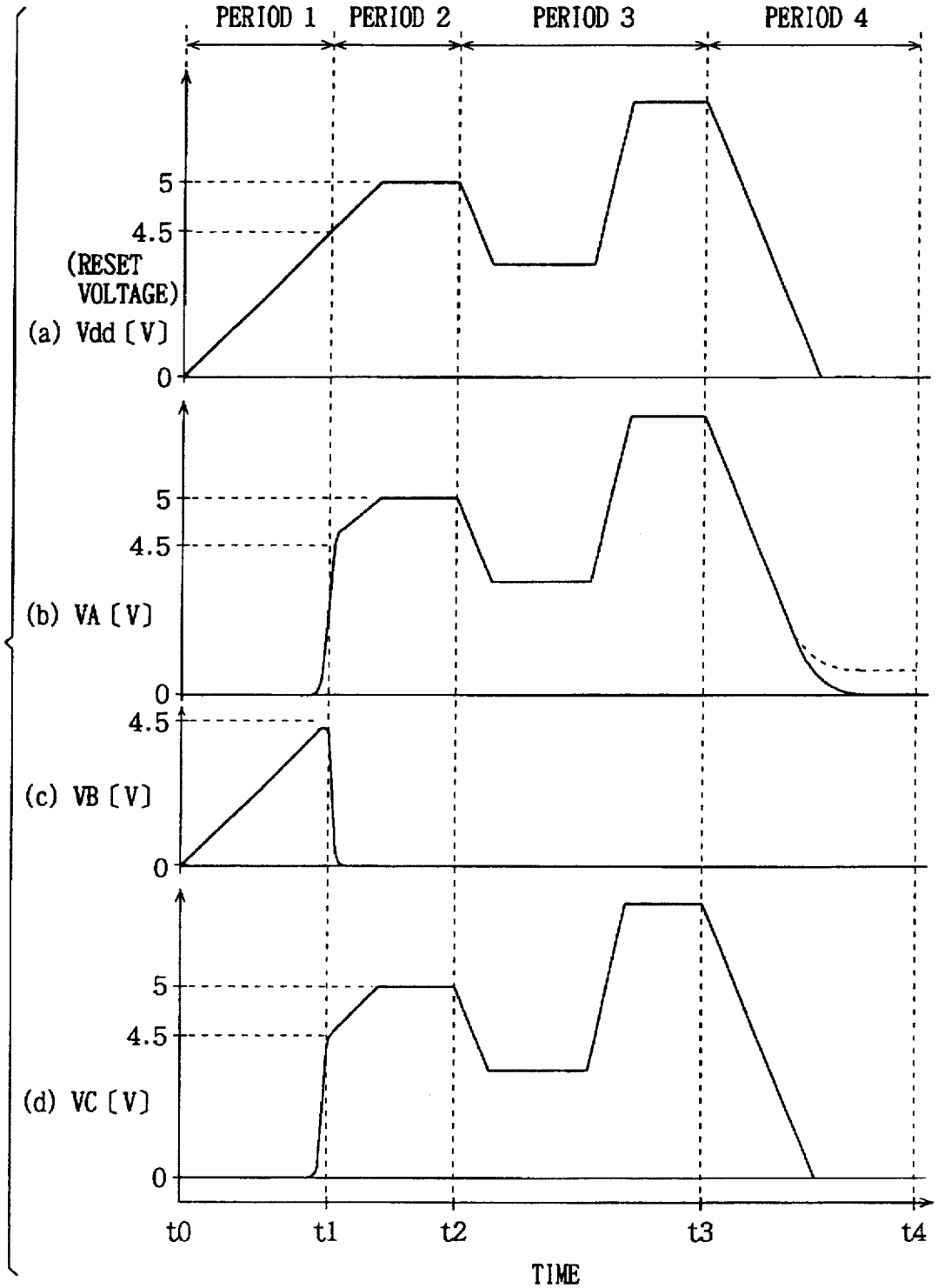

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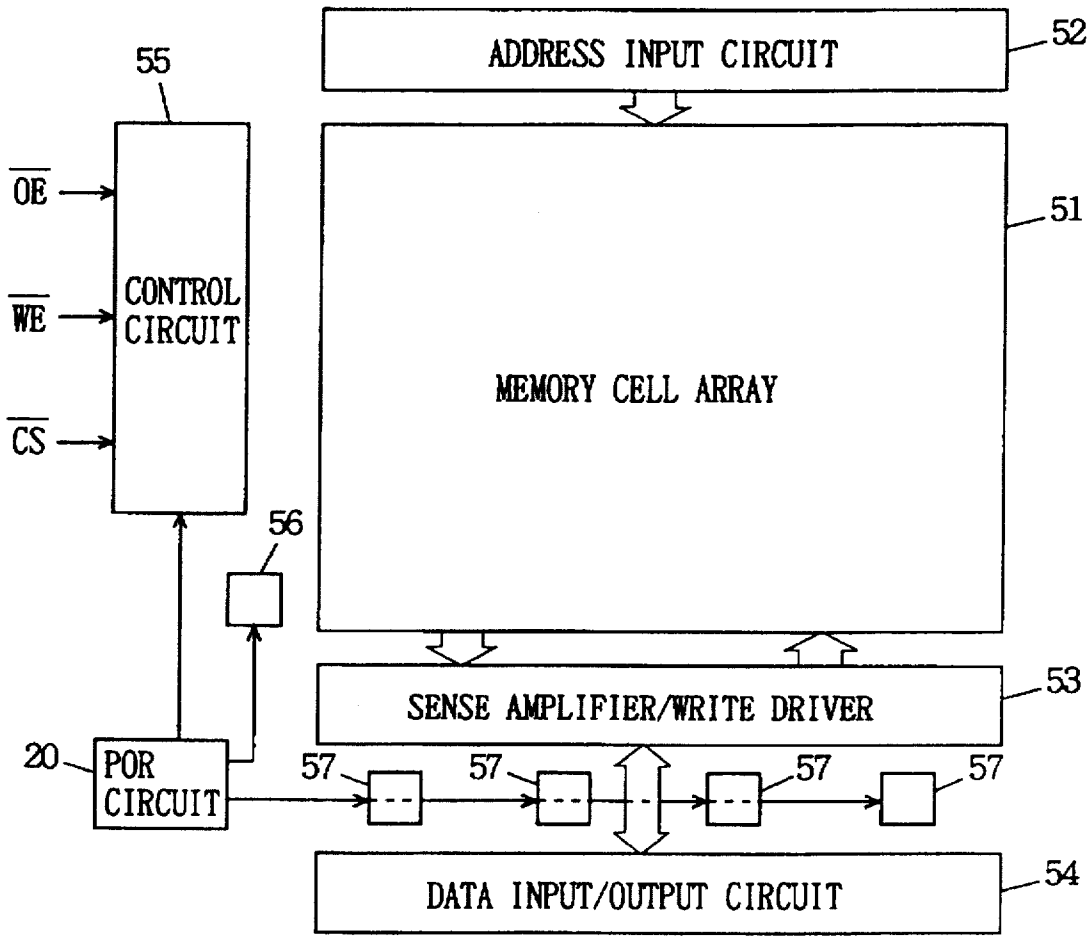
FIG. 5



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