

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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REALTEK SEMICONDUCTOR CORP.,  
Petitioner,

v.

ATI TECHNOLOGIES ULC,  
Patent Owner.

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IPR2023-00564  
Patent 7,742,053 B2

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Before JAMES P. CALVE, BRIAN J. McNAMARA, and  
KEVIN W. CHERRY, *Administrative Patent Judges*.

McNAMARA, *Administrative Patent Judge*.

DECISION  
Granting Institution of *Inter Partes* Review  
*35 U.S.C. § 314*

## I. INTRODUCTION

Realtek Semiconductor Corp. (“Petitioner”) filed a petition, Paper 1 (“Petition” or “Pet.”), to institute an *inter partes* review (“IPR”) of claims 1–9 (the “challenged claims”) of U.S. Patent No. 7,742,053 B2 (“the ’053 patent”). 35 U.S.C. § 311. ATI Technologies ULC (“Patent Owner”) filed a Preliminary Response, Paper 6 (“Prelim. Resp.”), contending that the Petition should be denied as to all challenged claims.

We have jurisdiction under 35 U.S.C. § 6. This Decision on Institution is issued pursuant to 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

A decision to institute under § 314 may not institute on fewer than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018). In addition, per Board practice, if the Board institutes trial, it will institute “on all of the challenged claims and on all grounds of unpatentability asserted for each claim.” *See* 37 C.F.R. § 42.108(a).

Having considered the arguments and the associated evidence presented in the Petition and the Preliminary Response, for the reasons described below, we institute *inter partes* review.

## II. REAL PARTIES IN INTEREST

The Petition identifies Petitioner Realtek Semiconductor Corp. as the real party-in-interest. Pet. 1. Patent Owner identifies ATI Technologies ULC as the real party-in-interest. Paper 4, 1.

### III. RELATED MATTERS

Petitioner and Patent Owner identify the following as proceedings that may affect or may be affected by a decision in this proceeding:

*Advanced Micro Devices, Inc. et al v. TCL Industries Holdings Co., Ltd. et al.*, C.A. No. 2:22-cv-00134 (E.D. Tex. May 5, 2022); and

*Certain Graphics Systems, Components Thereof, and Digital Televisions Containing The Same*, Inv. No. 337-TA-1318 (“ITC Investigation”)

Pet. 1–2; Paper 4, 1.

### IV. THE '053 PATENT

The '053 patent relates to graphic processing and the interleaving of arithmetic logic unit (ALU) operations with texture fetching operations. Ex. 1001, 1:16–18. According to the '053 patent, in a typical graphics processing system, the processing elements, such as vertices and/or pixels are processed through multiple steps that provide for the application of textures and other processing instructions, as done through one or more ALUs. *Id.* at 1:24–27. The '053 patent describes its Figure 1, reproduced below, as “a prior art sequencing system.” *Id.* at 1:32.

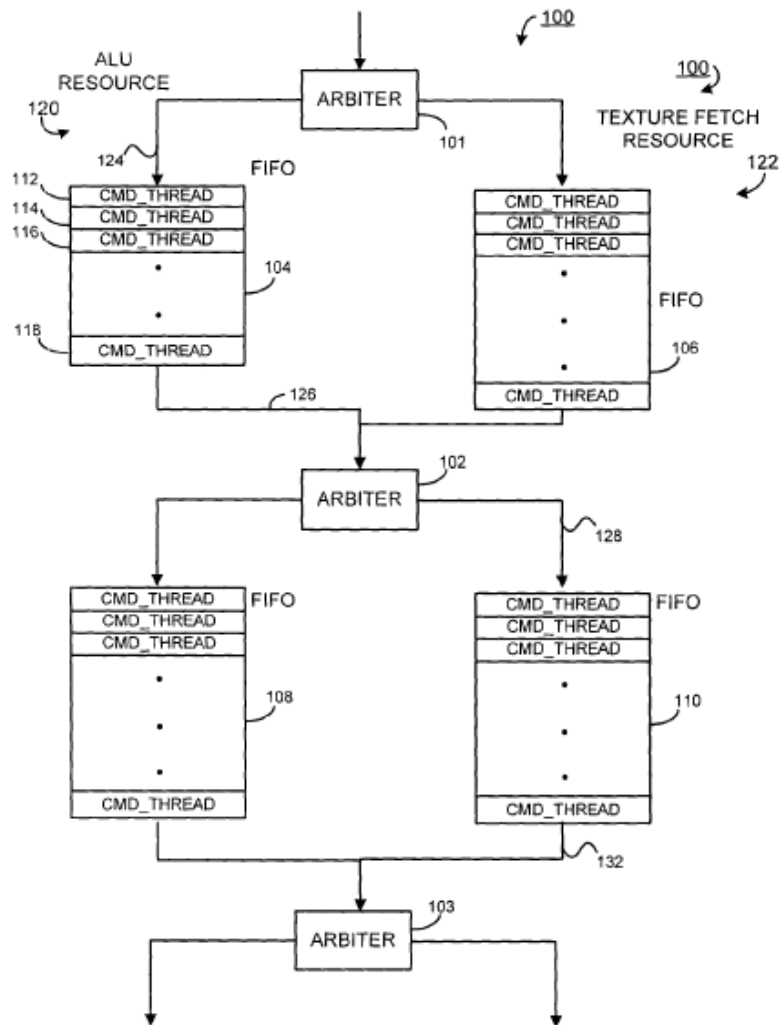


FIG. 1  
(PRIOR ART)

*Id.* at Fig. 1. In Figure 1, system 100 includes first, second and third arbiters 101–103 and multiple buffers or “reservation stations” 104, 106, 108, 110 that are typically first-in, first-out (FIFO) buffers. *Id.* at 1:33–35, 1:43–44, 1:46–47. Each buffer or reservation station stores multiple command threads, e.g., 112, 114, 116, 118. *Id.* at 1:36–38; *see also id.* at 2:37–41. “[A] command thread is a sequence of commands applicable to a corresponding element such as a pixel command thread relative to processing of pixel elements and a vertex command thread relative to vertex processing commands.” *Id.* at 2:41–45.

Prior art system 100 is divided into ALU resource division 120 and texture fetch resource division 122. Ex. 1001, 1:38–40. In ALU resource division 120, command thread 118 selected by arbiter 101 may be received in a reservation station 104, 108 from an input command 124; command thread 118 may then be withdrawn from reservation stations 104 and 108 and provided to an ALU (not shown). *Id.* at 1:40–45. Command threads within texture fetch resource division 122 may be withdrawn from reservation stations 106 and 110 to be provided to a texture fetch processor (not shown). *Id.* at 1:45–48. First buffer 104 receives input command 124 and outputs a completed command thread 126 to second arbiter 102. *Id.* at 1:49–51. Arbiter 102 receives input command 124 and in due course provides the command thread to either an appropriate texture fetch buffer 110 or an ALU buffer 108. *Id.* at 1:55–57. The steps are repeated where an output thread command 128 is provided to another ALU (not shown) or texture fetch processor (not shown) and returned to buffer 108 or 110. *Id.* at 1:57–61. Buffer 110 also produces output 132 which is a command thread that may be provided to another arbiter 103 to be provided further along the graphics processing pipeline. *Id.* at 1:61–64.

According to the '053 patent, the prior art system in Figure 1 is inflexible because delineated ALU resource buffers and texture fetch resource buffers are such that command threads must be sequentially provided through the various buffers 104, 106, 108, and 110; the system also does not support an unlimited number of dependent fetches based on the buffer structure and their connectivity between each other and the available ALU resources and texture fetch resources. Ex. 1001, 1:65–2:6.

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