US011061682B2

(12) **United States Patent**
Vorbach

(10) **Patent No.: US 11,061,682 B2**
(45) **Date of Patent: Jul. 13, 2021**

(54) **ADVANCED PROCESSOR ARCHITECTURE**

(71) Applicants: **Martin Vorbach**, Lingenfeld (DE); **Hyperion Core, Inc.**, Los Gatos, CA (US)

(72) Inventor: **Martin Vorbach**, Lingenfeld (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **15/535,697**

(22) PCT Filed: **Dec. 13, 2015**

(86) PCT No.: **PCT/US2015/065418**
§ 371 (c)(1),
(2) Date: **Jun. 13, 2017**

(87) PCT Pub. No.: **WO2016/100142**
PCT Pub. Date: **Jun. 23, 2016**

(65) **Prior Publication Data**

US 2018/0004530 A1 Jan. 4, 2018

(30) **Foreign Application Priority Data**

Dec. 15, 2014 (EP) 14197929
Jun. 24, 2015 (EP) 150201036

(51) **Int. Cl.**
G06F 9/38 (2018.01)
G06F 9/30 (2018.01)
G06F 9/32 (2018.01)

(52) **U.S. Cl.**
CPC ***G06F 9/3855*** (2013.01); ***G06F 9/3001*** (2013.01); ***G06F 9/3017*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC G06F 9/3855
See application file for complete search history.

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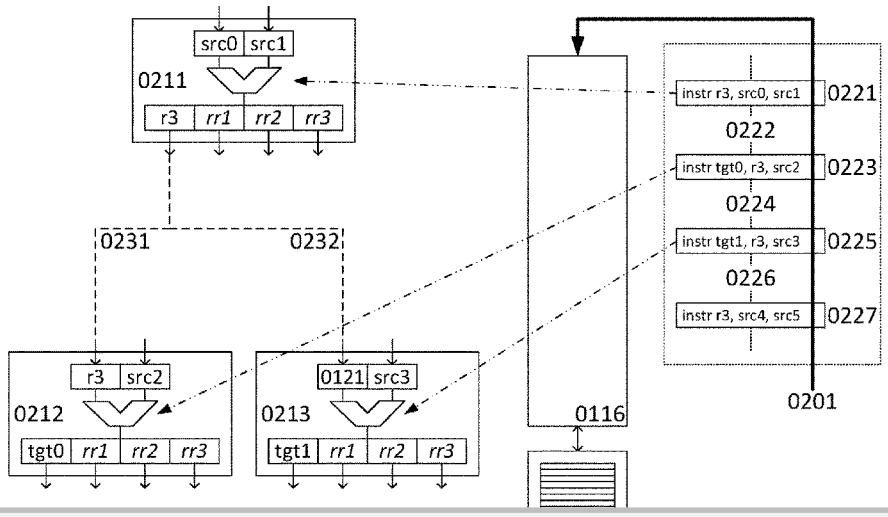
Primary Examiner — Michael J Metzger
(74) *Attorney, Agent, or Firm* — IP Spring

(57) **ABSTRACT**

The invention relates to a method for processing instructions out-of-order on a processor comprising an arrangement of execution units. The inventive method comprises looking up operand sources in a Register Positioning Table and setting operand input references of the instruction to be issued accordingly, checking for an Execution Unit (EXU) available for receiving a new instruction, and issuing the instruction to the available Execution Unit and entering a reference of the result register addressed by the instruction to be issued to the Execution Unit into the Register Positioning Table (RPT).

20 Claims, 26 Drawing Sheets



(52) **U.S. Cl.**
CPC ***G06F 9/30065*** (2013.01); ***G06F 9/30098*** (2013.01); ***G06F 9/325*** (2013.01); ***G06F 9/327*** (2013.01); ***G06F 9/382*** (2013.01); ***G06F 9/384*** (2013.01); ***G06F 9/3824*** (2013.01); ***G06F 9/3826*** (2013.01); ***G06F 9/3828*** (2013.01); ***G06F 9/3836*** (2013.01); ***G06F 9/3842*** (2013.01); ***G06F 9/3844*** (2013.01); ***G06F 9/3846*** (2013.01); ***G06F 9/3848*** (2013.01); ***G06F 9/3857*** (2013.01); ***G06F 9/3861*** (2013.01); ***G06F 9/3863*** (2013.01); ***G06F 9/3885*** (2013.01)

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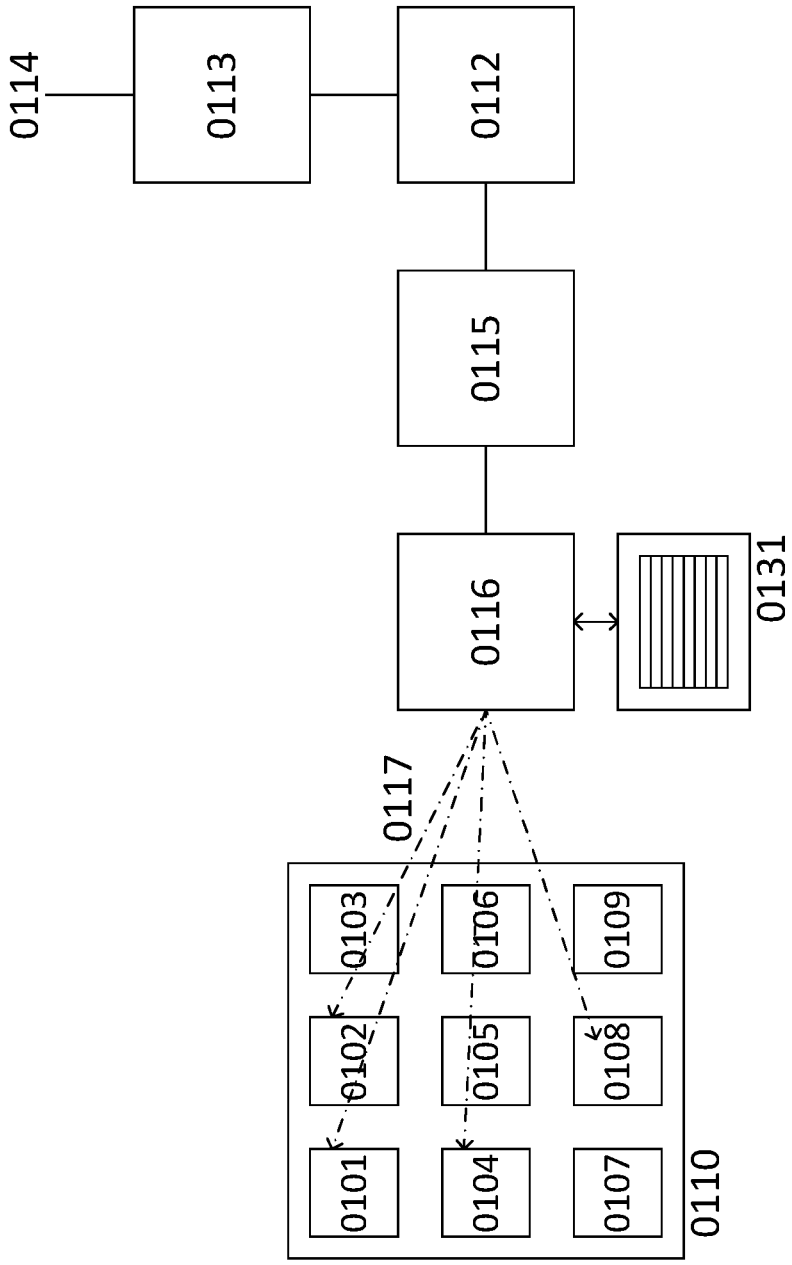
Fig. 1



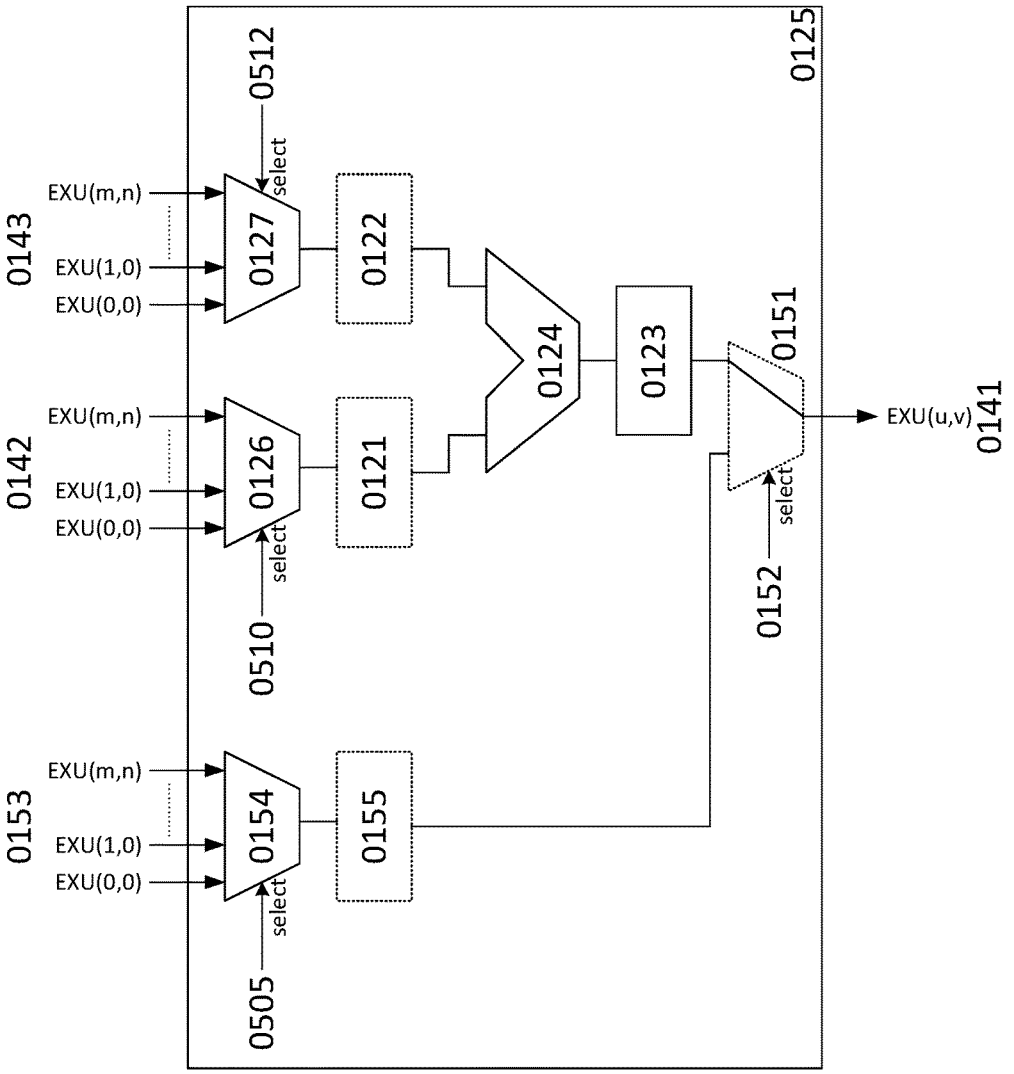


Fig. 1A

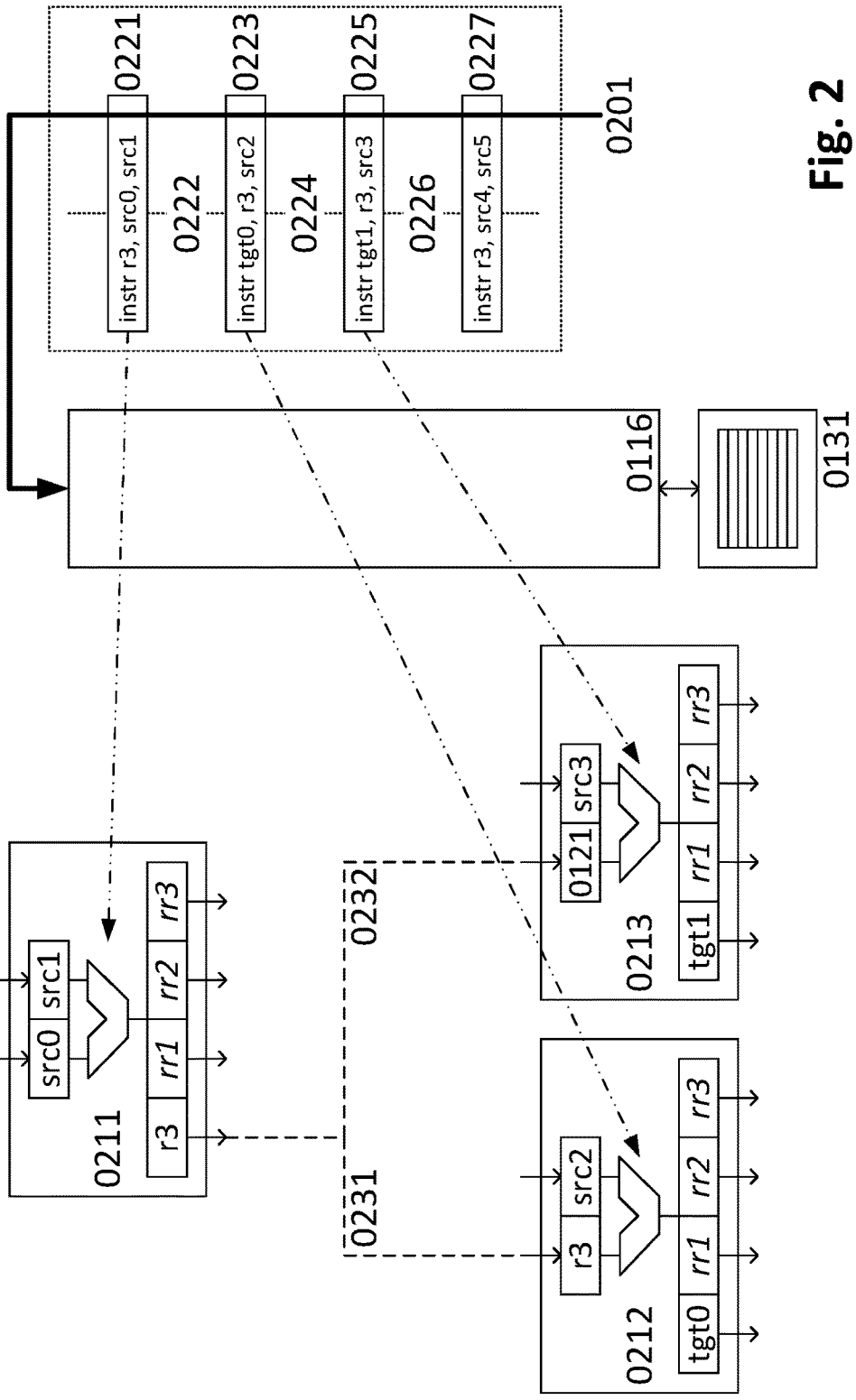


Fig. 2

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