UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE PATENT TRIAL AND APPEAL BOARD LENOVO (UNITED STATES) INC. Petitioner v. INTELLECTUAL VENTURES II LLC Patent Owner Case No. IPR2024-01226

DECLARATION OF R. JACOB BAKER, P.E., PH.D. IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,646,835 B1

Patent No. 7,646,835 B1



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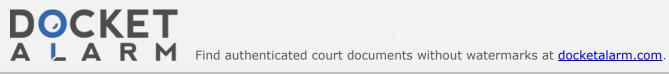
	1. Johnson (Ex. 1004)43
	2. Jeddeloh (Ex. 1005)
	3. Keeth (Ex. 1006)
Е.	Summary of the Grounds
F.	Ground 1: Claims 1-23 are Obvious Over <i>Johnson</i> in View of <i>Jeddeloh</i>
	1. Claim 1
	2. Claim 2 – The method of claim 1, wherein the integrated circuit device comprises a DRAM component
	3. Claim 3 – The method of claim 2, wherein said altering is performed by a memory controller coupled to the DRAM component. 97
	4. Claim 4 – The method of claim 2, wherein the DRAM component comprises a DDR DRAM component
	5. Claim 5 – The method of claim 4, wherein the data signals comprise a plurality of data bus (DQ) signals for the DDR DRAM component
	6. Claim 6 – The method of claim 5, wherein the sampling signals comprise a plurality of sampling bus (DQS) signals for the DDR DRAM component
	7. Claim 7
	8. Claim 8 – The system of claim 7, wherein the integrated circuit device comprises a DRAM component
	9. Claim 9 – The system of claim 8, wherein the DRAM component comprises a DDR DRAM component
	10. Claim 10 – The system of claim 9, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component. 124



11. Claim 11 – The system of claim 10, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component. 125
12. Claim 12
13. Claim 13
14. Claim 14 – The method of claim 13, wherein said performing a coarse calibration comprises simultaneously varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal by a five percent step increase 134
15. Claim 15 – The method of claim 13, wherein said performing a fine calibration comprises varying each of the phase shift of the command signal, the phase shift of the data signal, and the phase shift of the sampling signal one at a time by a two percent step increase.136
16. Claim 16 – The method of claim 13, further comprising configuring the memory controller to operate the DRAM component in the optimal operating mode
17. Claim 17 – The method of claim 12, wherein the DRAM component comprises a DDR DRAM component
18. Claim 18 – The method of claim 17, wherein the data signals comprise a plurality of DQ signals for the DDR DRAM component. 140
19. Claim 19 – The method of claim 18, wherein the sampling signals comprise a plurality of DQS signals for the DDR DRAM component
20. Claim 20
21. Claim 21
22. Claim 22 – The computer readable media of claim 21, wherein the method further comprises configuring the memory controller to operate the DRAM component in the optimal operating mode 146
23. Claim 23



	G.	Ground 2: Claims 1-3, 7-8, and 12 are Obvious Over <i>Johnson</i> in View of <i>Keeth</i>
		1. Claim 1
		2. Claim 2 – The method of claim 1, wherein the integrated circuit device comprises a DRAM component
		3. Claim 3 – The method of claim 2, wherein said altering is performed by a memory controller coupled to the DRAM component. 166
		7. Claim 7
		8. Claim 8 – The system of claim 7, wherein the integrated circuit device comprises a DRAM component
		12. Claim 12
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