

(12) **United States Patent**
Johnson et al.

(10) **Patent No.:** **US 6,434,081 B1**
 (45) **Date of Patent:** **Aug. 13, 2002**

(54) **CALIBRATION TECHNIQUE FOR MEMORY DEVICES**

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(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/570,481**

(22) Filed: **May 12, 2000**

(51) **Int. Cl.**⁷ **G11C 8/00**

(52) **U.S. Cl.** **365/233; 365/187.07; 365/194**

(58) **Field of Search** **365/233, 189.05, 365/189.07, 189.08, 194, 230.08**

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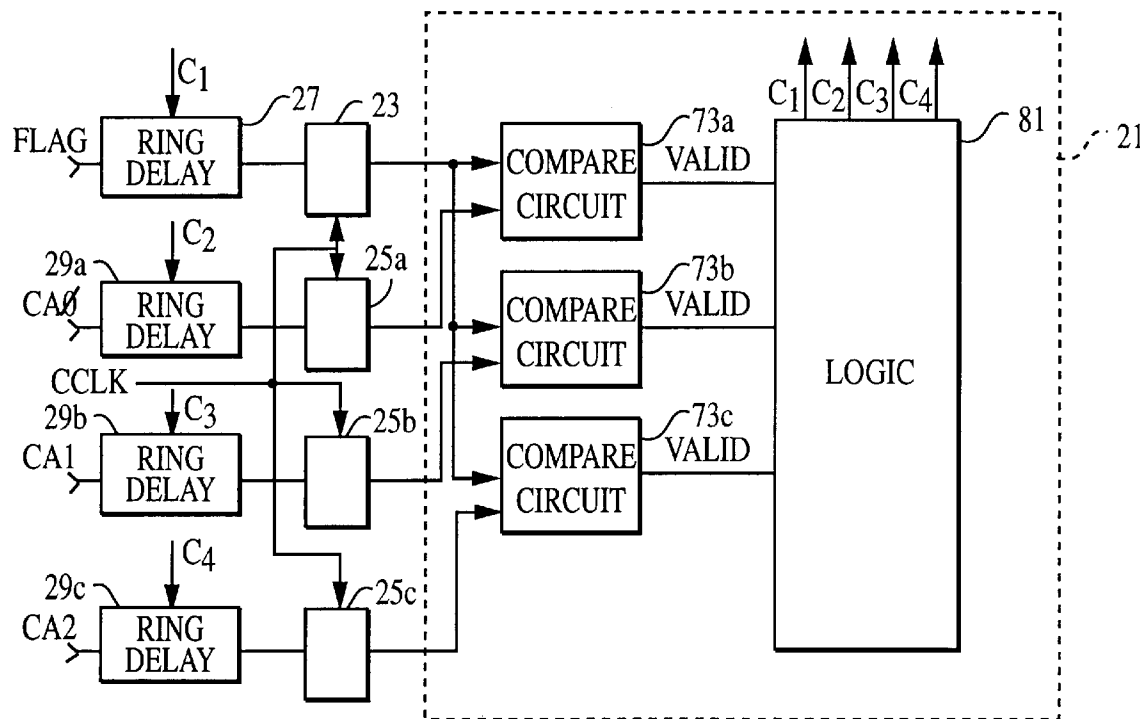
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(57) **ABSTRACT**

Disclosed is an improved start-up/reset calibration apparatus and method for use in a memory device. One of a plurality of data paths is bit wise calibrated relative to a clock signal and thereafter others of the plurality of data paths are bit wise aligned to a previously calibrated data path to produce serial and parallel bit alignment on all data paths.

104 Claims, 8 Drawing Sheets



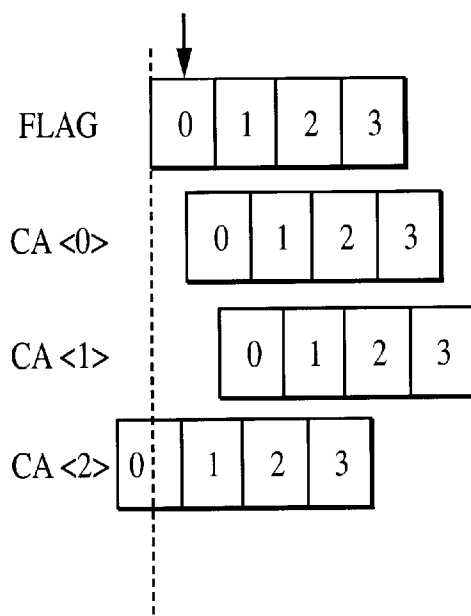


FIG. 1
PRIOR ART

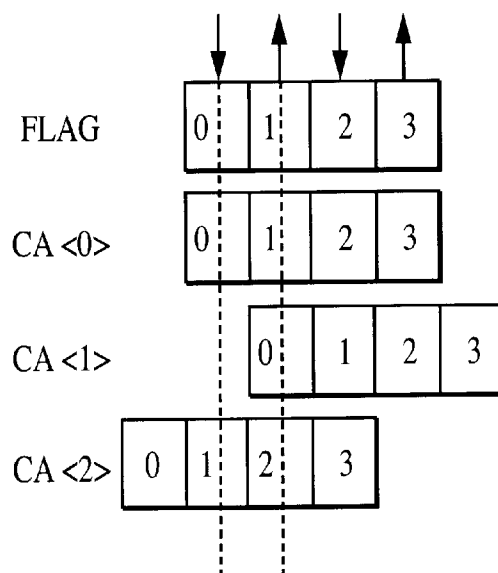


FIG. 2
PRIOR ART

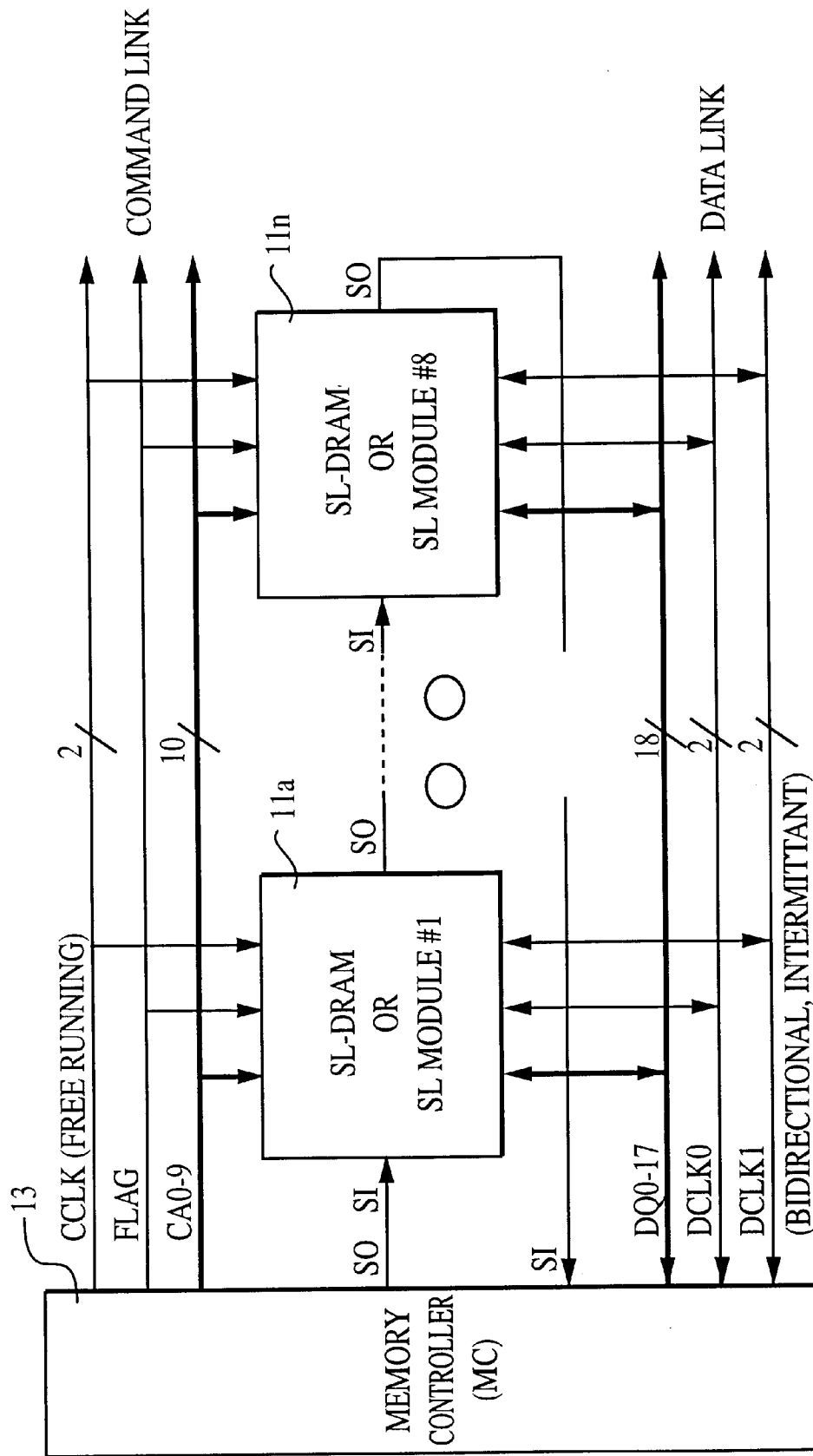


FIG. 3

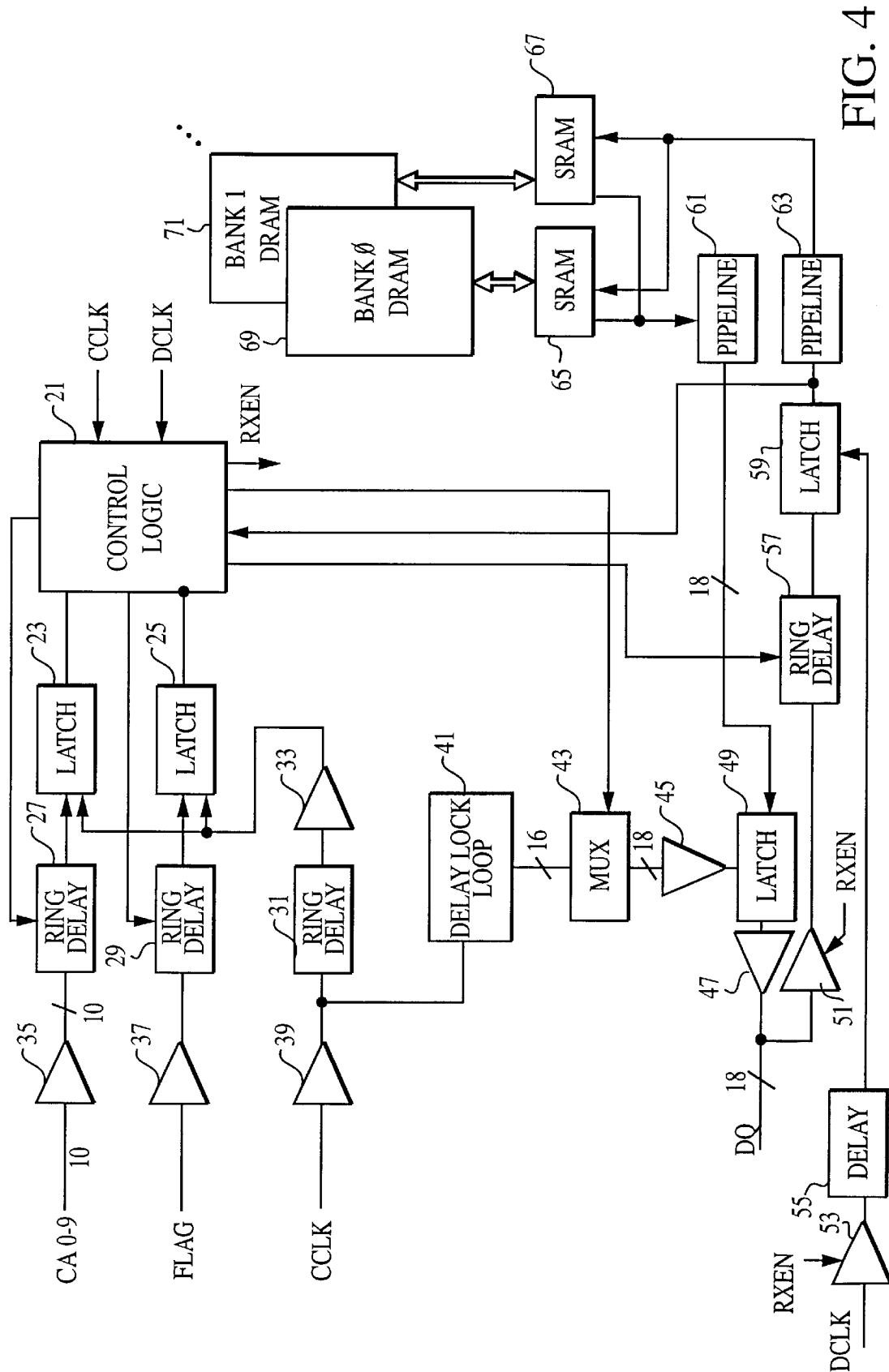


FIG. 4

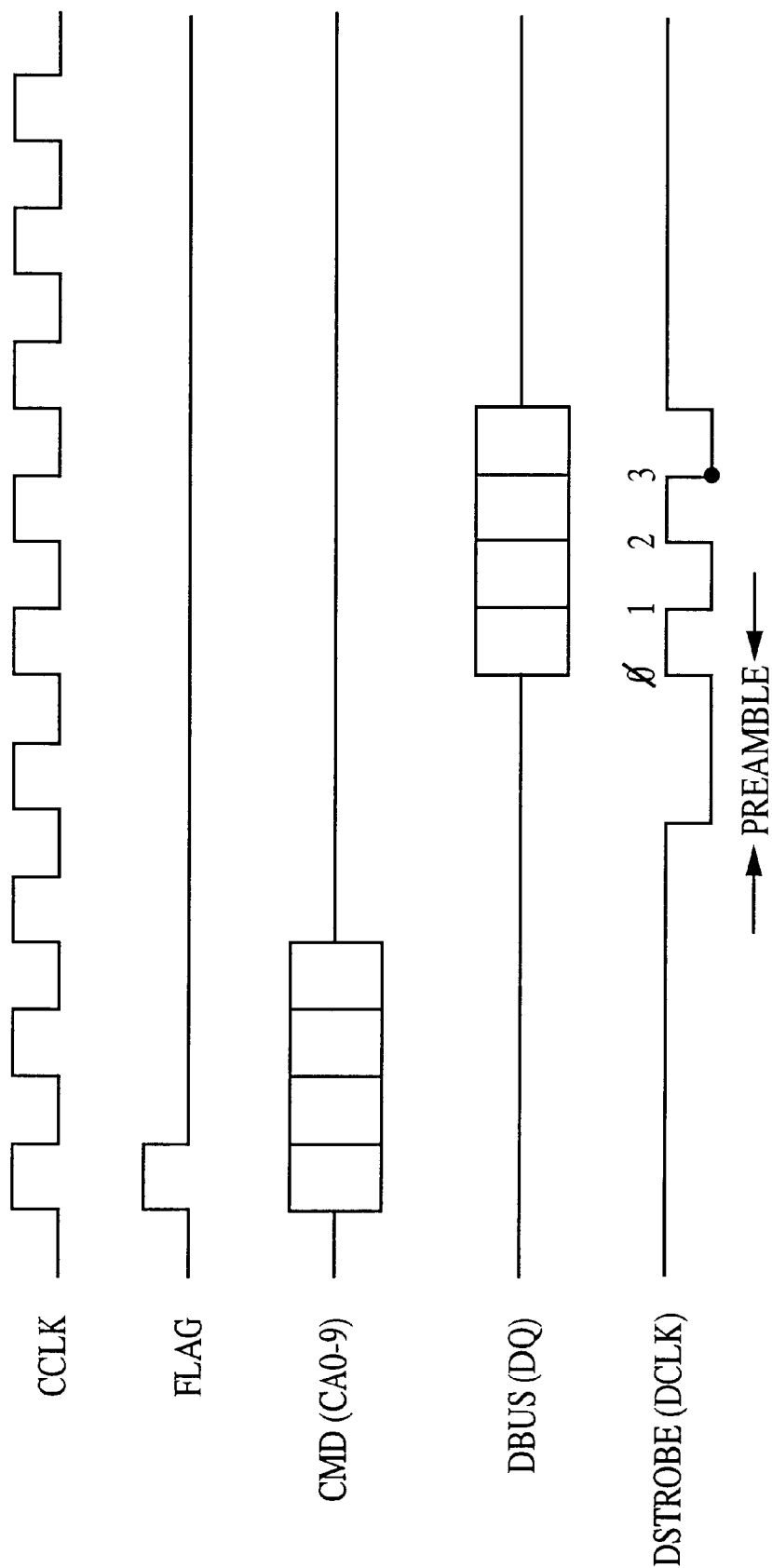


FIG. 5

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