

(12) **United States Patent**
Jeddeloh(10) **Patent No.:** **US 6,629,222 B1**
(45) **Date of Patent:** ***Sep. 30, 2003**(54) **APPARATUS FOR SYNCHRONIZING STROBE AND DATA SIGNALS RECEIVED FROM A RAM**(75) Inventor: **Joseph M. Jeddeloh**, Minneapolis, MN (US)(73) Assignee: **Micron Technology Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/352,719**(22) Filed: **Jul. 13, 1999**(51) Int. Cl.⁷ **G06F 12/00; G06F 13/00**(52) U.S. Cl. **711/167; 711/104; 713/401; 365/193; 365/194**(58) **Field of Search** **711/104, 167; 710/52-53, 240, 58-59; 365/193-194, 233, 189.05; 713/400-401**(56) **References Cited****U.S. PATENT DOCUMENTS**

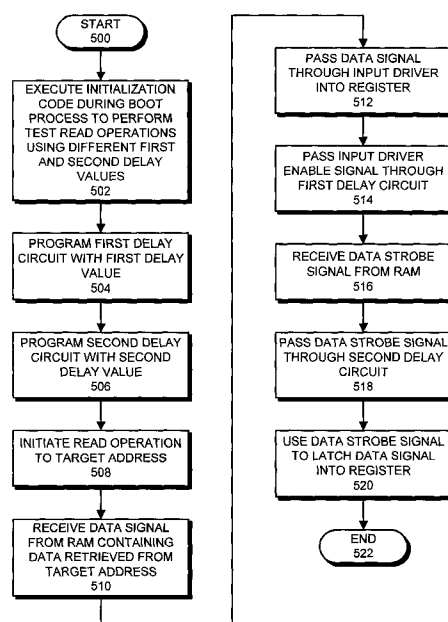
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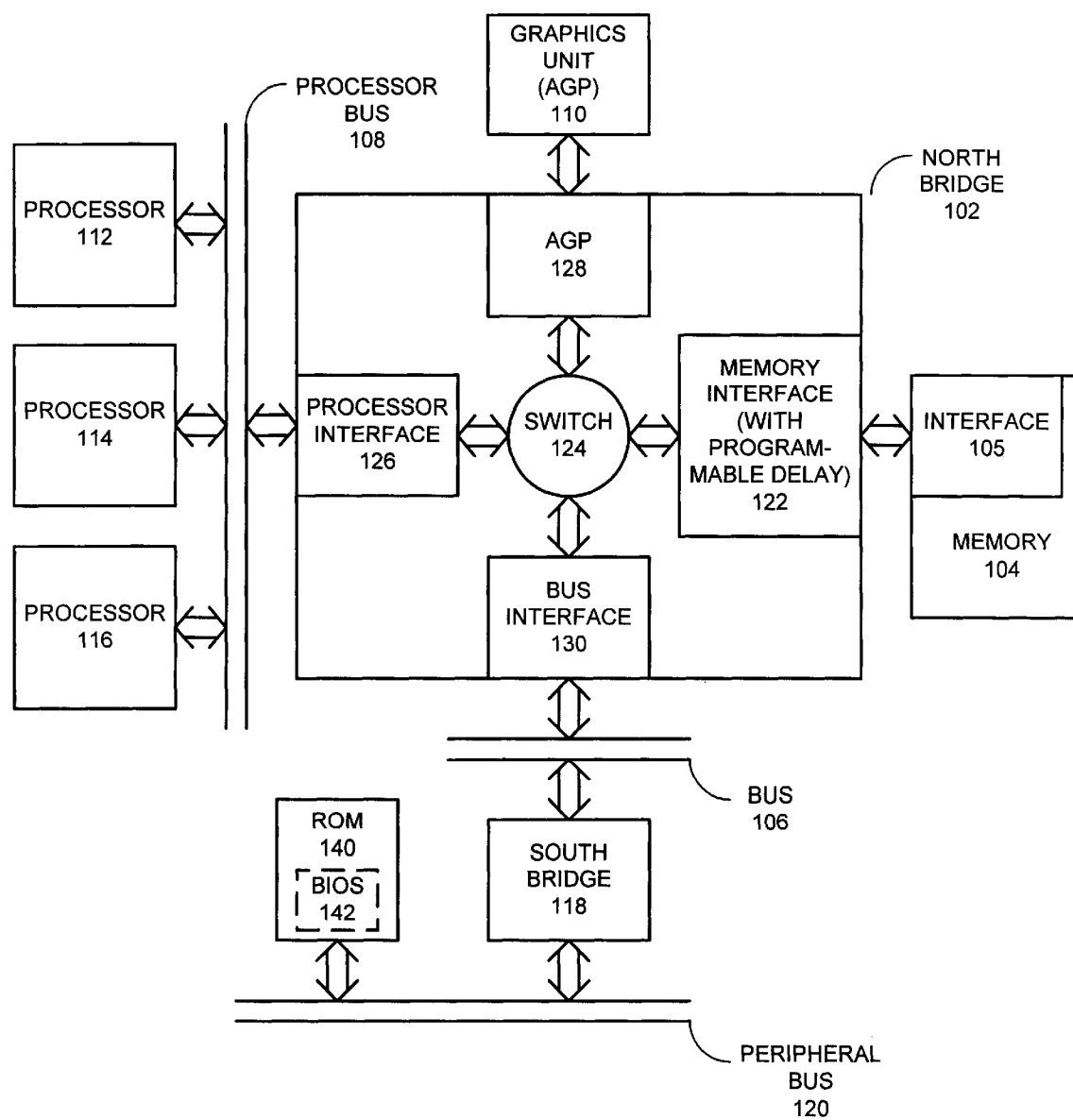
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Primary Examiner—Reginald G. Bragdon*Assistant Examiner*—Pierre M. Vital(74) *Attorney, Agent, or Firm*—Park, Vaughan & Fleming LLP(57) **ABSTRACT**

One embodiment of the present invention provides an apparatus that synchronizes a data signal and a data strobe signal received from a random access memory. This apparatus includes a mechanism that initiates a read operation to the random access memory by sending a target address for the read operation to the random access memory. The apparatus also includes an input driver that receives the data signal containing data retrieved from the target address from the random access memory. Coupled to the input driver is a register that stores the data signal. A first programmable delay circuit is coupled to an enable input of the input driver in order to synchronize the driving of the input driver with the data signal received from the random access memory. A second programmable delay circuit is coupled between the data strobe signal and a clock input of the register. This second programmable delay circuit is configured to delay the data strobe signal so as to synchronize the data strobe signal with the data signal received from the random access memory. One embodiment of the present invention includes an initialization mechanism that determines the first delay value and the second delay value by performing test read operations using a plurality of different combinations of different first delay values and different second delay values. In a variation on this embodiment, this initialization mechanism includes code executed during a system boot process that determines the first delay value and the second delay value.

18 Claims, 6 Drawing Sheets

**FIG. 1**

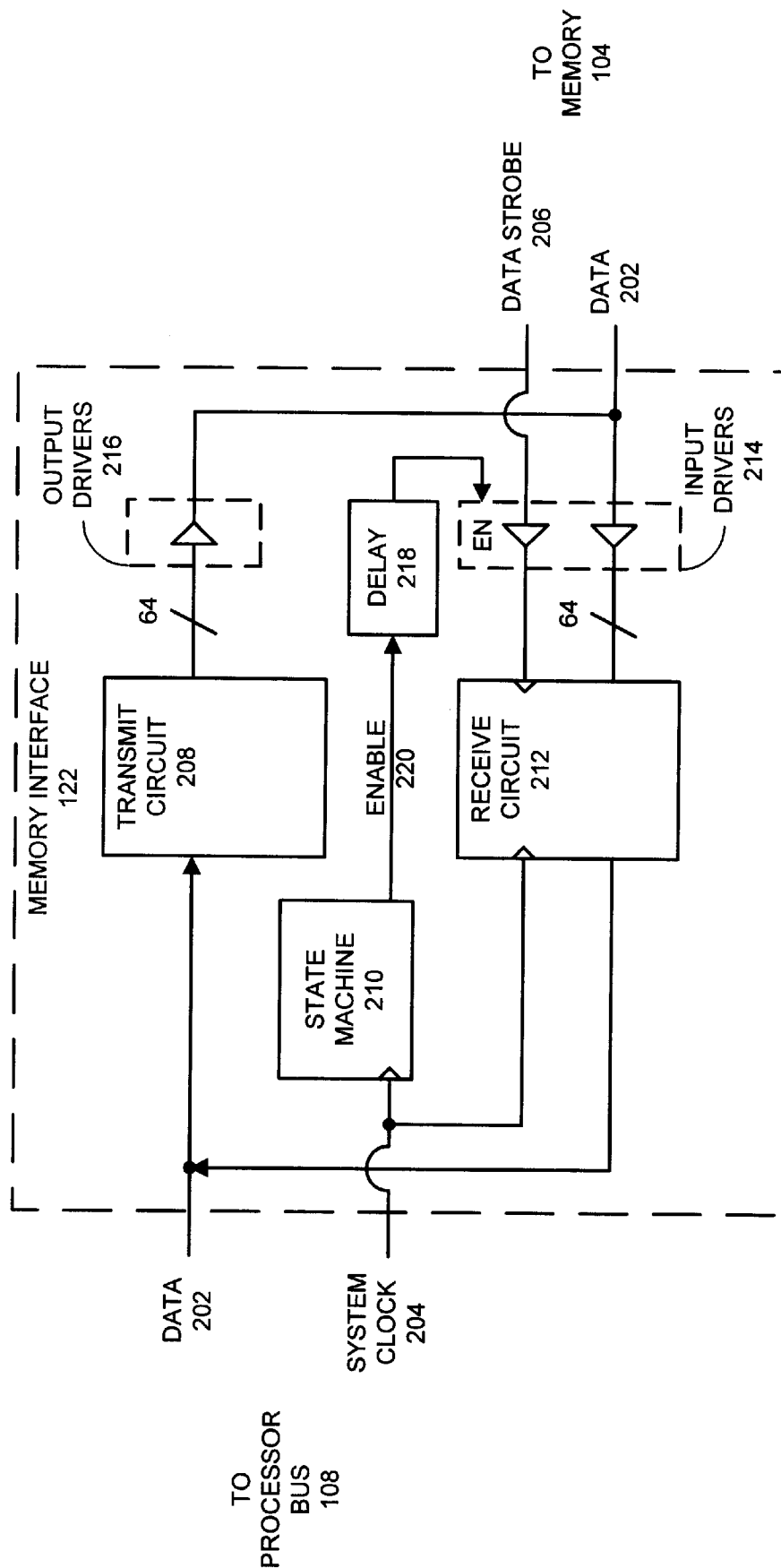


FIG. 2

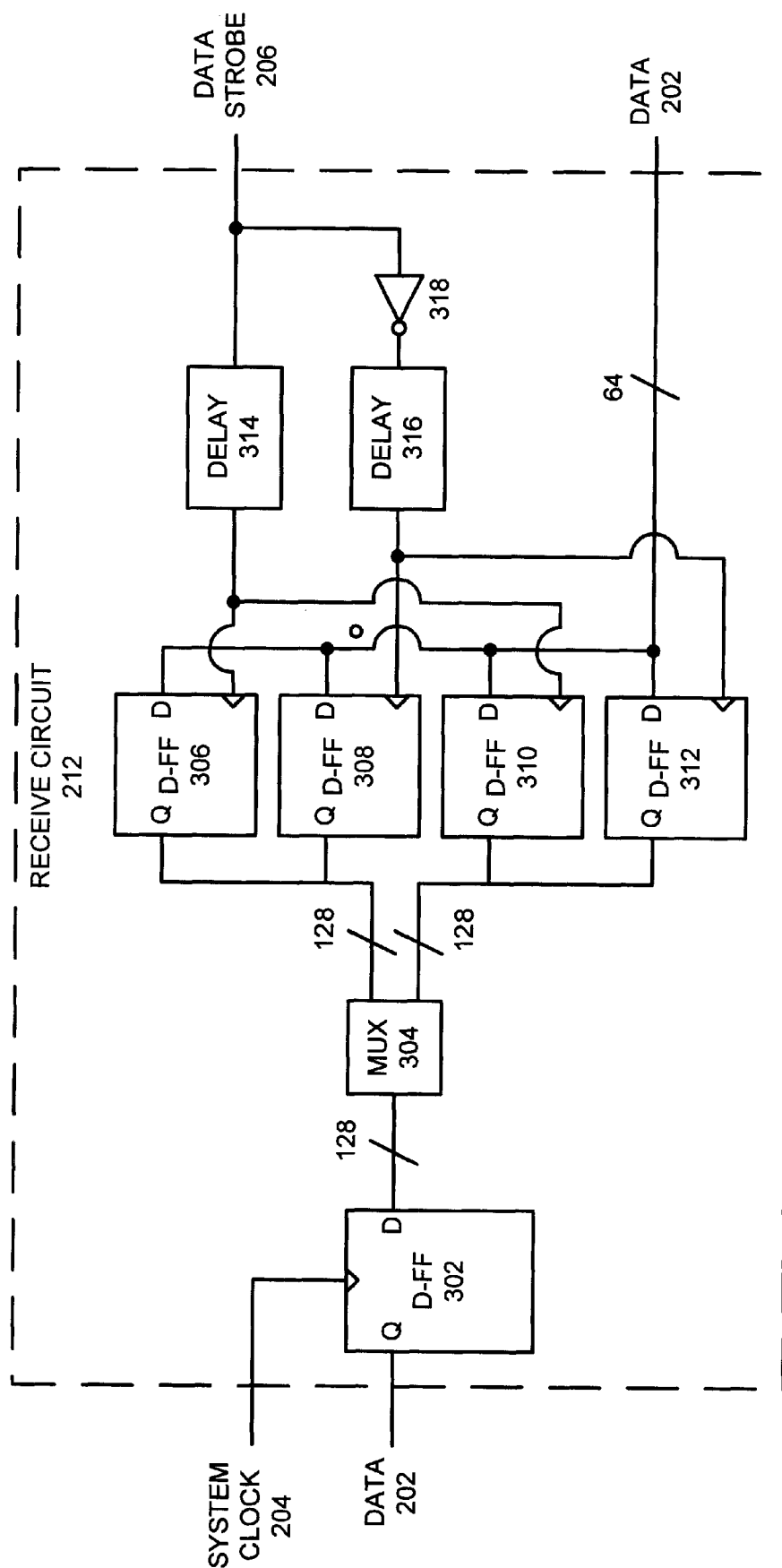


FIG. 3

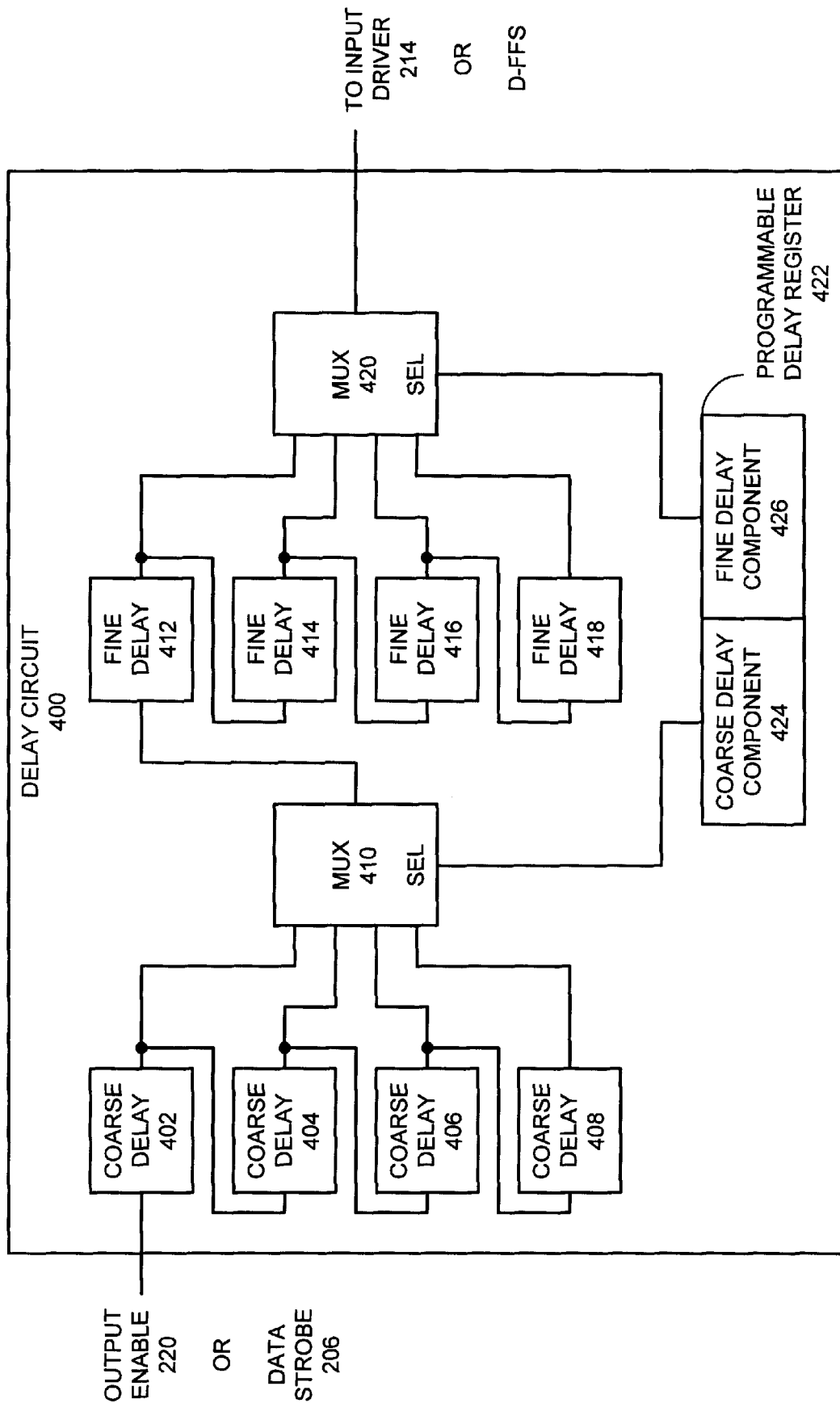


FIG. 4

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