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United States Patent [19]

Keeth

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[54] **CLOCK VERNIER ADJUSTMENT**

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[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

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[51] **Int. Cl.**[7] **G11C 8/00**

[52] **U.S. Cl.** **365/233**; 365/194; 327/202

[58] **Field of Search** 365/233, 194; 327/202, 218

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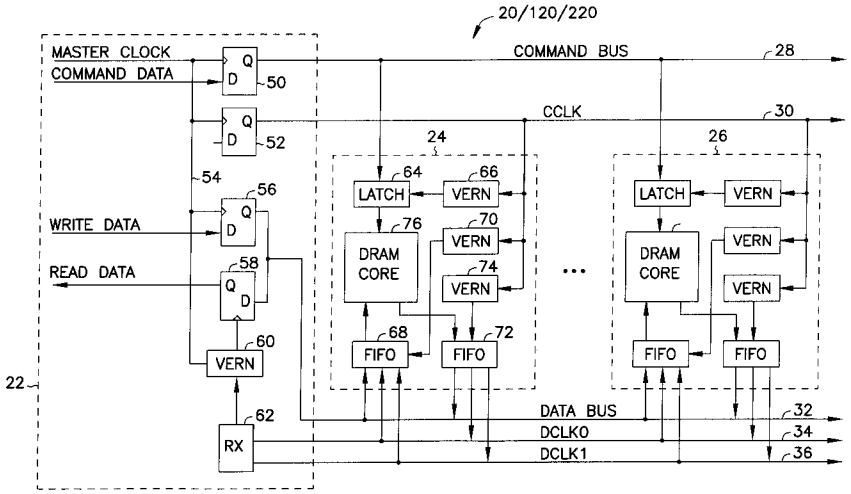
[57] **ABSTRACT**

A integrated circuit, such as a memory integrated circuit, includes a vernier clock adjustment circuit receiving an input clock signal and providing a rising-edge clock signal representing the input clock signal delayed by a rising-edge delay and providing a falling-edge clock signal representing the input clock signal delayed by a falling-edge delay. An edge triggered circuit receives data and the rising-edge and falling-edge clock signals, and stores data at the rising-edge of the rising-edge clock signal and at the falling-edge of the falling-edge clock signal. One form of the invention is a memory system having a memory controller coupled to memory modules through data and command busses. Each memory module includes the vernier clock adjustment circuitry.

6 Claims, 9 Drawing Sheets



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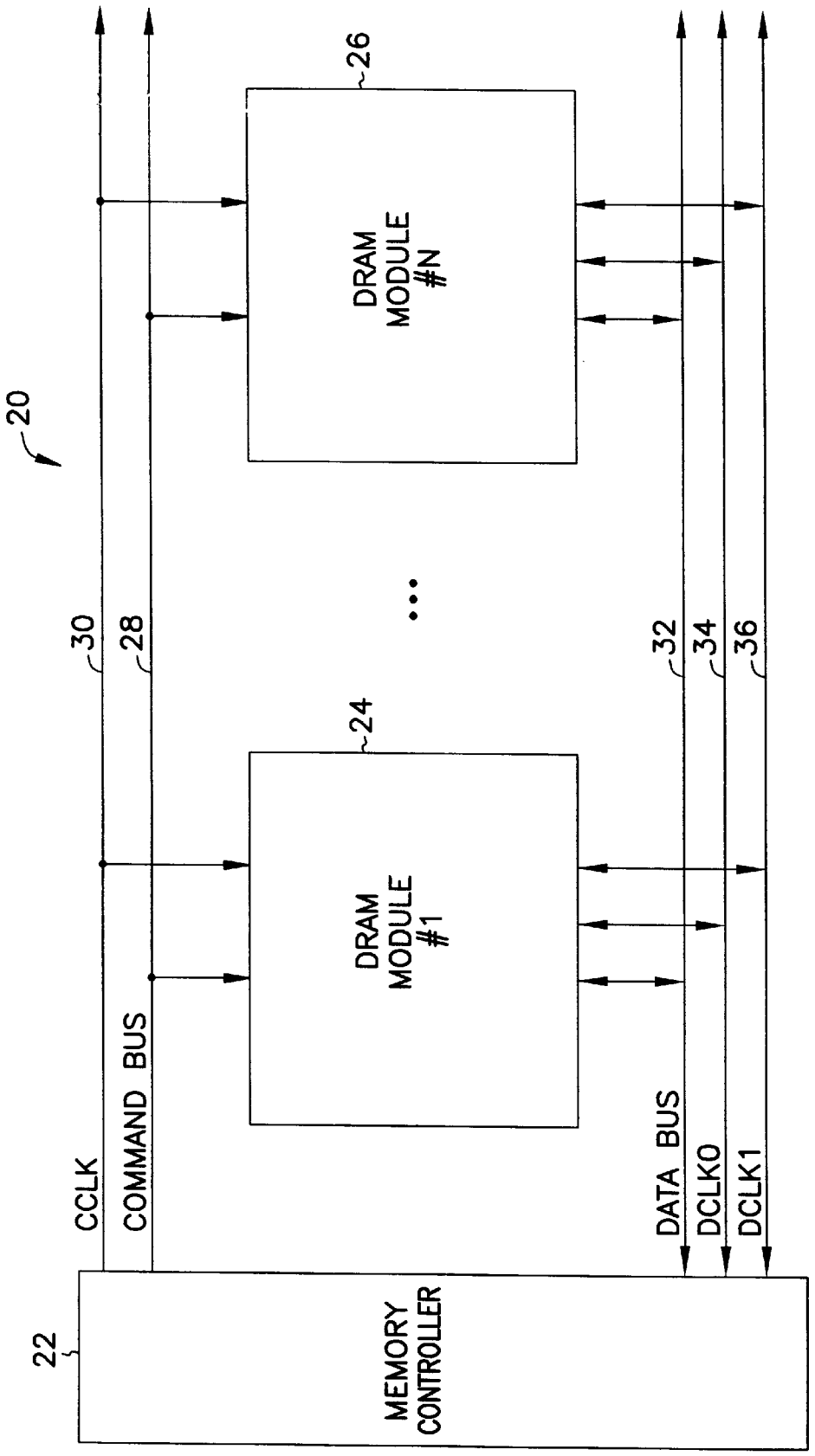

FIG. 1

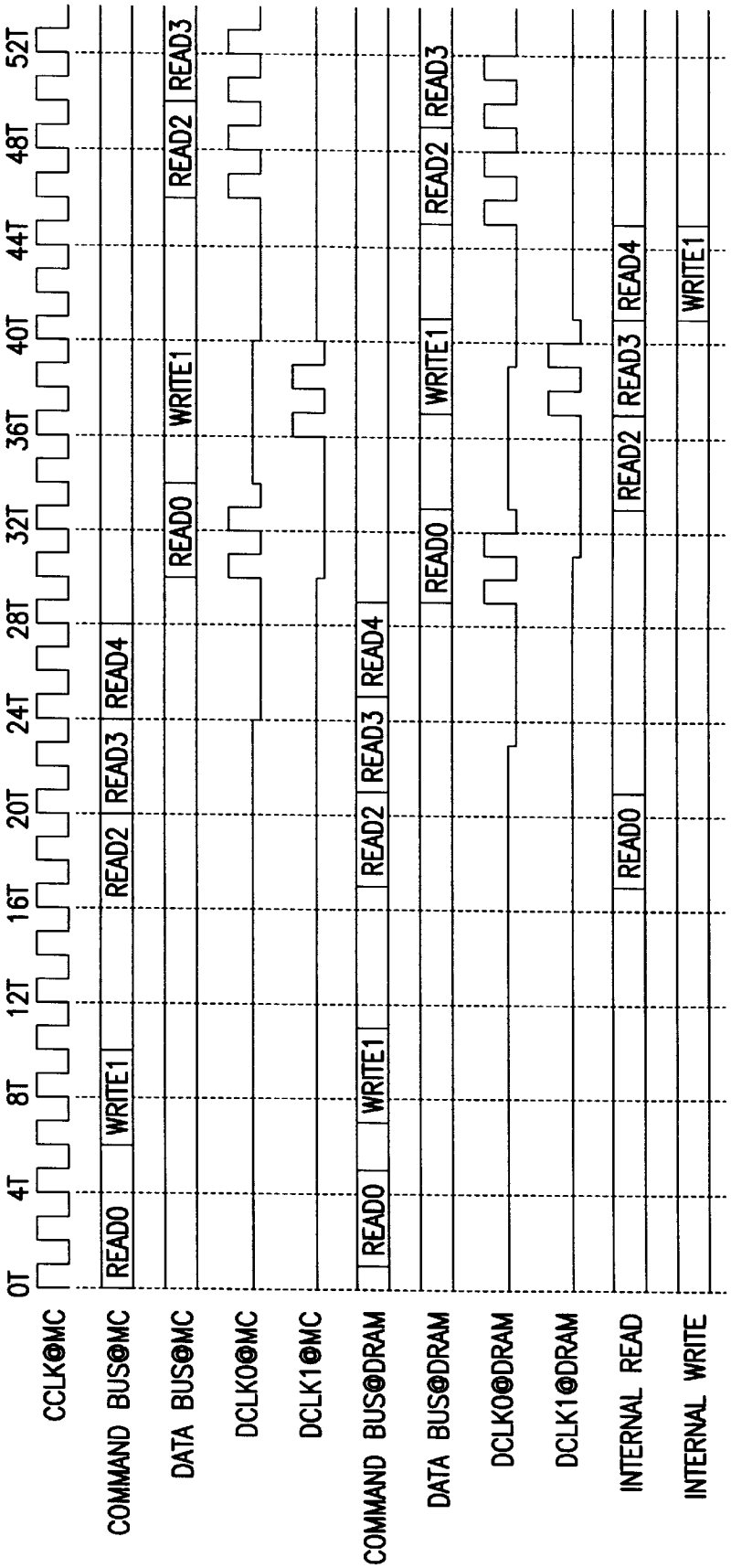

FIG. 2

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