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Double Data Rate (DDR) SDRAM Specification

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Double Data Rate (DDR) SDRAM Specification

(The material contained in this standard was formulated under the cognizance of the JC-42.3 Subcommittee on RAM Memories and approved by the JEDEC Board of Directors. The text in this standard is from the following BoD Ballots: JCB-99-70, JCB-99-84, JCB-00-08, JCB-00-10 JCB-00-11, JCB-00-12, JCB-00-13, and JCB-00-23.)

1 Purpose

To define the minimum set of requirements for JEDEC-compliant 64M x4/x8/x16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

2 Scope

This comprehensive standard defines all required aspects of 64M x4/x8/x16 DDR SDRAMs, including features, functionality, AC and DC parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well.

DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION

16 M x4 (4 M x4 x4 banks), 8 M x8 (2 M x8 x4 banks), 4 M x16 (1 M x16 x4 banks)

FEATURES

- Double–data–rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge–aligned with data for READs; center–aligned with data for WRITEs
- Differential clock inputs (CK and $\overline{CK}$)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 2, 4, or 8
- CAS Latency: 2 or 2.5
- AUTO PRECHARGE option for each burst access
- Auto Refresh and Self Refresh Modes
- 15.6 μs Maximum Average Periodic Refresh Interval
- 2.5 V (SSTL_2 compatible) I/O
- VDDQ = +2.5 V ±0.2 V
- VDD = +3.3 V ±0.3 V or +2.5 V ±0.2 V

GENERAL DESCRIPTION

The 64 Mb DDR SDRAM is a high–speed CMOS, dynamic random–access memory containing 67,108,864 bits. It is internally configured as a quad–bank DRAM.

The 64 Mb DDR SDRAM uses a double–data–rate architecture to achieve high–speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 64 Mb DDR SDRAM effectively consists of a single 2n–bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n–bit wide, one–half–clock–cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge–aligned with data for READs and center–aligned with data for WRITEs.

The 64 Mb DDR SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going HIGH and $\overline{CK}$ going LOW will be referred to as the postive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable read or write burst lengths of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self–timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power–saving, power–down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Initial devices will have a VDD supply of 3.3 V (nominal). Eventually, all devices will migrate to a VDD supply of 2.5 V (nominal). During this initial period of product availability, this split will be vendor and device specific.

This data sheet includes all features and functionality required for JEDEC DDR devices; options not required, but listed, are noted as such. Certain vendors may elect to offer a superset of this specification by offering improved timing and/or including optional features. Users benefit from knowing that any system design based on the required aspects of this specification are supported by all DDR SDRAM vendors; conversely, users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

Note: The functionality described in, and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Note: This specification defines the minimum set of requirements for JEDEC 64 M x4/x8/x16 DDR SDRAMs. Vendors will provide individual data sheets in their specific format. Vendor data sheets should be consulted for optional features or superset specifications.

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