UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.
Petitioner

v.

INTELLECTUAL VENTURES II LLC
Patent Owner

Case No. IPR2024-01226
Patent No. 7,646,835 B1

DECLARATION OF DUNCAN BAUSERMAN IN SUPPORT OF PETITION

I, Duncan Bauserman, make the following declaration pursuant to 28 U.S.C. § 1746:

1. I am a patent agent at the law firm of Bookoff McAndrews PLLC.

2. I provide this Declaration in connection with the above-identified *Inter Partes* Review proceeding requested at the United States Patent and Trademark Office by Lenovo (United States) Inc. against Intellectual Ventures II LLC under 35 U.S.C. § 311, 37 C.F.R. § 42.104. Unless otherwise stated, the facts stated in this Declaration are based on my personal knowledge.

3. Exhibit 1008 is a true and correct copy of *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* by Bruce L. Jacob, published in December of 2002, which I personally downloaded online from the website https://user.eng.umd.edu/~blj/CS-590.26/references/DRAM-Systems.pdf on July 25, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

4. Exhibit 1009 is a true and correct copy of *RAM Guide Part I: DRAM and SDRAM Basics* by Jon Stokes, published in July of 2000, which I personally downloaded online from the website https://arstechnica.com/gadgets/2000/07/ram-guide-part1-1/5/ on July 25, 2024. An exhibit label on the first page and page

numbers on all pages have been added to the bottom of this document but no other alterations have been made.

5. Exhibit 1010 is a true and correct copy of *Design and PCB Layout Considerations for Dynamic Memories Interfaced to the Z80 CPU* by Tim Olmstead, published in October of 1996, which I personally downloaded online from the website http://www.cpm.z80.de/download/dram.pdf on July 25, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

6. Exhibit 1011 is a true and correct copy of *A Performance Comparison of Contemporary DRAM Architectures* by Vinodh Cuppu *et al.*, published in May of 1999), which I personally downloaded online from the website https://dl.acm.org/doi/pdf/10.1145/300979.300998 on July 25, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

7. Exhibit 1012 is a true and correct copy of *How to Use DDR SDRAM* by Elpida Memory, published in April of 2002, which I personally downloaded online from the website https://www.sjalander.com/research/thesis/pdf/ref6.pdf on July 25, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

8. Exhibit 1013 is a true and correct copy of *Hyundai Electronics Actively Supplying DDR SDRAM Modules to Major PC Makers* by SK hynix, published in March of 2001, which I personally downloaded online from the website https://news.skhynix.com/hyundai-electronics-actively-supplying-ddr-sdram-modules-to-major-pc-makers/ on July 25, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

9. Exhibit 1014 is a true and correct copy of *SLDRAM: High Performance, Open-Standard Memory* by Peter Gillingham *et al.*, published in December of 1997, which I personally downloaded online from the website https://www.ardent-tool.com/CPU/docs/AMD/anatomy/misc/articles/gillingh.pdf on July 25, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

10. Exhibit 1015 is a true and correct copy of *3.1. How Memory Works with the Processor* by Technick, published in March of 1998, which I personally downloaded online from the website https://technick.net/guides/hardware/umg/03_001/ on July 25, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

11. Exhibit 1016 is a true and correct copy of *Memory Access Scheduling* by Scott Rixner *et al.*, published in March of 2000, which I personally downloaded online from the website http://cva.stanford.edu/publications/2000/mas.pdf on July 31, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

12. Exhibit 1017 is a true and correct copy of *Computer-System Operation,* published in July of 1999 (last visited July 25, 2024), which I personally downloaded online from the website https://www.slawinski.ca/courses/CS-30/unit2/part1.htm on July 25, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

13. Exhibit 1018 is a true and correct copy of *Course-to-fine Estimation of Visual Motion* by Eero P. Simoncelli, published in September of 1993, which I personally downloaded online from the website https://www.cns.nyu.edu/pub/eero/simoncelli93d.pdf on July 25, 2024. An exhibit label on the first page and page numbers on all pages have been added to the bottom of this document but no other alterations have been made.

14. Exhibit 1019 is a true and correct copy of excerpts from *Modern Dictionary of Electronics Seventh Edition* by Rudolf F. Graf, published in February of 1999,

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