



US005304996A

United States Patent [19][11] **Patent Number:** **5,304,996****Hsu et al.**[45] **Date of Patent:** **Apr. 19, 1994**

[54] **8B/10B ENCODER PROVIDING ONE OF PAIR OF NONCOMPLEMENTARY, OPPOSITE DISPARITY CODES RESPONSIVE TO RUNNING DISPARITY AND SELECTED COMMANDS**

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[73] **Assignee:** **Advanced Micro Devices, Inc., Sunnyvale, Calif.**

[21] **Appl. No.:** **839,604**

[22] **Filed:** **Feb. 21, 1992**

[51] **Int. Cl.⁵** **H03M 7/00**

[52] **U.S. Cl.** **341/95; 341/58**

[58] **Field of Search** **341/58, 68, 95**

[56] **References Cited****U.S. PATENT DOCUMENTS**

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[57] **ABSTRACT**

An 8B/10B encoder which provides an output of one of a pair of opposite disparity non-complementary 8B/10B command code outputs responsive to RD and selected command inputs.

11 Claims, 3 Drawing Sheets

93		97	96	95	94
Command	TX Command Input	TX Command Input 4-Bit Binary	PRD	Encoded NRZ Sub-Block	ARD
		$C_3 C_2 C_1 C_0$	—	abcdei fghi	
0	K28.0	0000	—	001111 0100	—
1	K28.1	0001	—	001111 1001	+
2	K28.2	0010	—	001111 0101	+
3	K28.3	0011	—	001111 0011	+
4	K28.4	0100	—	001111 0010	—
5	K28.5	0101	—	001111 1010	+
6	K28.6	0110	—	001111 0110	+
7	K28.7	0111	—	001111 1000	—
8	K23.7	1000	—	111010 1000	—
9	K27.7	1001	—	110110 1000	—
10	K29.7	1010	—	101110 1000	—
11	K30.7	1011	—	011110 1000	—
12	Reserved	1100	d —	001111 1010	+
13	K28.5+	1101	d —	001111 1010	+
14	D21.5/4	1110	—	101010 1010	—
15	D10.5/4	1111	—	010101 1010	—
0	K28.0	0000	+	110000 1011	+
1	K28.1	0001	+	110000 0110	—
2	K28.2	0010	+	110000 1010	—
3	K28.3	0011	+	110000 1100	—
4	K28.4	0100	+	110000 1101	+
5	K28.5	0101	+	110000 0101	—
6	K28.6	0110	+	110000 1001	—
7	K28.7	0111	+	110000 0111	+
8	K23.7	1000	+	000101 0111	+
9	K27.7	1001	+	001001 0111	+
10	K29.7	1010	+	010001 0111	+
11	K30.7	1011	+	100001 0111	+
12	Reserved	1100	+	001111 1010	+
13	K28.5+	1101	+	001111 1010	+
14	D21.5/4	1110	+	101010 0010	—
15	D10.5/4	1111	+	010101 0010	—

}98

}99

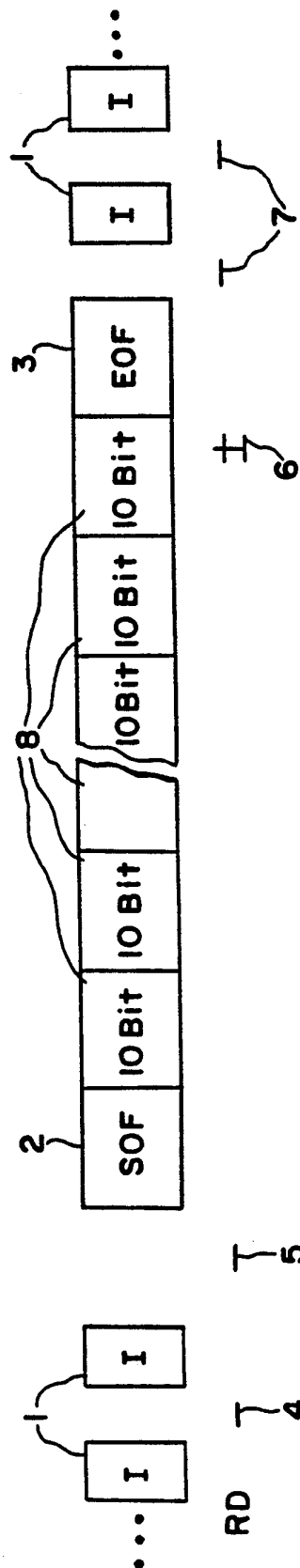
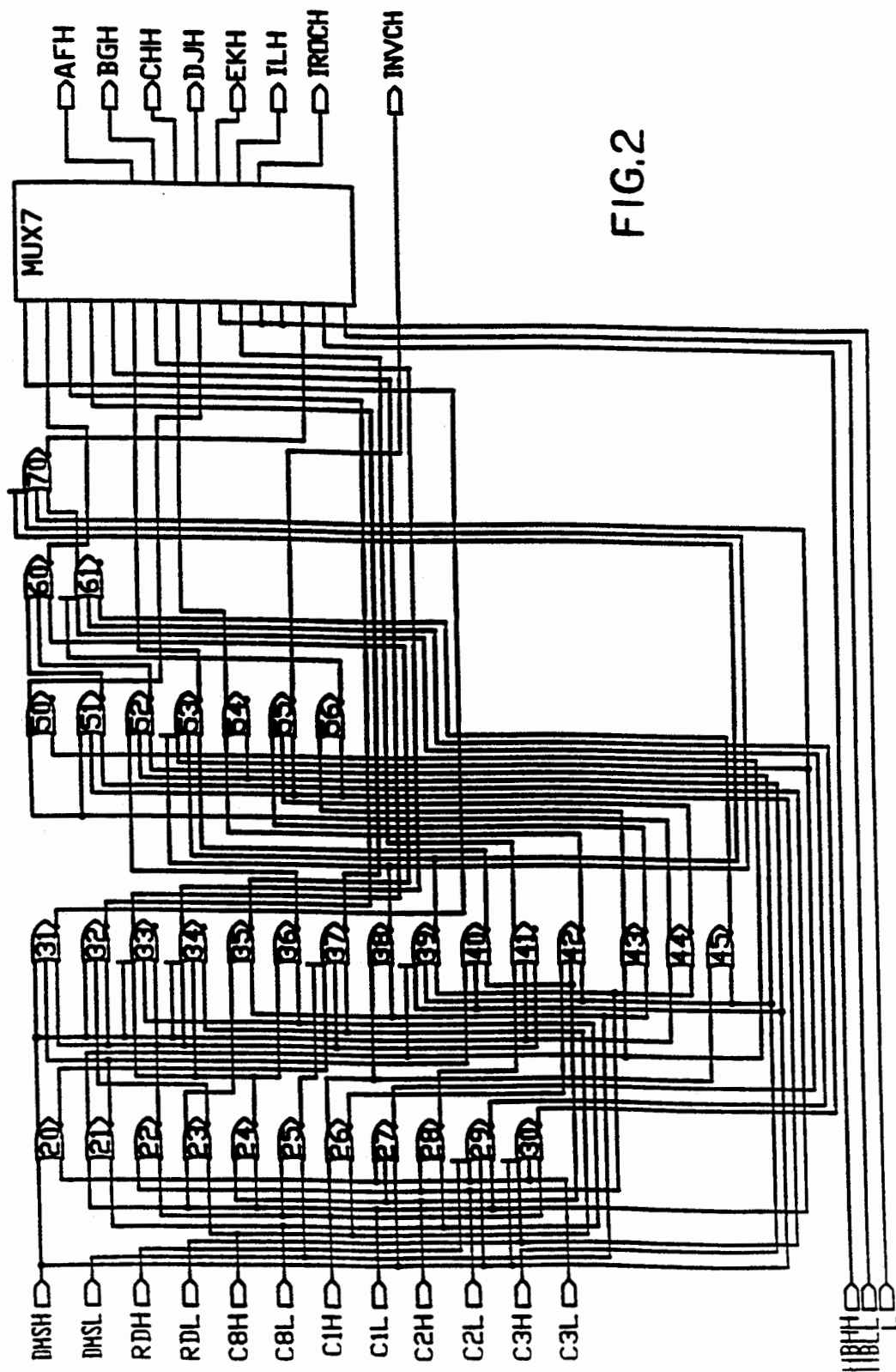


FIG. 1



93		97		96	95	94
Command	TX Command Input	TX Command Input 4-Bit Binary	PRD	Encoded NRZ Sub-Block		ARD
		$C_3 C_2 C_1 C_0$		abcdei	fghi	
0	K28.0	0000	-	001111	0100	-
1	K28.1	0001	-	001111	1001	+
2	K28.2	0010	-	001111	0101	+
3	K28.3	0011	-	001111	0011	+
4	K28.4	0100	-	001111	0010	-
5	K28.5	0101	-	001111	1010	+
6	K28.6	0110	-	001111	0110	+
7	K28.7	0111	-	001111	1000	-
8	K23.7	1000	-	111010	1000	-
9	K27.7	1001	-	110110	1000	-
10	K29.7	1010	-	101110	1000	-
11	K30.7	1011	-	011110	1000	-
12	Reserved	1100	d -	001111	1010	+
13	K28.5+	1101	d -	001111	1010	+
14	D21.5/4	1110	-	101010	1010	-
15	D10.5/4	1111	-	010101	1010	-
0	K28.0	0000	+	110000	1011	+
1	K28.1	0001	+	110000	0110	-
2	K28.2	0010	+	110000	1010	-
3	K28.3	0011	+	110000	1100	-
4	K28.4	0100	+	110000	1101	+
5	K28.5	0101	+	110000	0101	-
6	K28.6	0110	+	110000	1001	-
7	K28.7	0111	+	110000	0111	+
8	K23.7	1000	+	000101	0111	+
9	K27.7	1001	+	001001	0111	+
10	K29.7	1010	+	010001	0111	+
11	K30.7	1011	+	100001	0111	+
12	Reserved	1100	+	001111	1010	+
13	K28.5+	1101	+	001111	1010	+
14	D21.5/4	1110	+	101010	0010	-
15	D10.5/4	1111	+	010101	0010	-

FIG. 3

8B/10B ENCODER PROVIDING ONE OF PAIR OF NONCOMPLEMENTARY, OPPOSITE DISPARITY CODES RESPONSIVE TO RUNNING DISPARITY AND SELECTED COMMANDS

FIELD OF THE INVENTION

This invention relates to encoders and more particularly to 8B/10B encoders for high speed data transmission.

BACKGROUND OF THE INVENTION

High data rate transmission requires special encoding considerations to provide a high level of confidence that the transmitted data is being accurately reproduced at the receiver. The so called 8B/10B code is one type of encoding for serial data transmission which has become standard after adoption by ANSI X3T9.3 Fibre Channel Working Group. The code and equipment are described by Widmer et al in "A DC-Balanced Partitioned-Block, 8B/10B Transmission Code," *IBM Journal of Research and Development*, Volume 27, 1983, pp. 446-451.

Among other characteristics, the 8B/10B code satisfies the DC balance requirement which means that the coded transmission has a time averaged zero DC level. DC balance simplifies transmitter and receiver design and improves precision of the system. To accomplish this objective the 8B/10B code provides a unique way to encode 8 bit raw data blocks into 10 bit code words where the 10 bit code words are selected to maximize the number of binary data transitions. The high transition rate improves the ability of the receiver to stay locked in synchronism with the transmitter.

An important aspect of the 8B/10B code is the implementation of the concept called "running disparity" (RD). The running disparity is the cumulative sum of the disparity of all previously transmitted data blocks, where the disparity is defined as the difference between the number of ones and zeroes in a fixed size transmission block. The 8B/10B code does not use, as valid code bytes, all the 1024 bytes in the 2^{10} space. Only those bytes with a disparity of +2, 0, or -2 are valid.

By limiting the allowable RD during data transmission to -1 or +1, a simple scheme is enabled such that: a code word with zero disparity can be sent regardless of current RD;

a code word with +2 disparity can be sent only if current RD is -1; and

a code word with -2 disparity can be sent only if current RD is +1.

A related patent application, filed concurrently with the instant application, discloses "Method and Apparatus for Performing Running Disparity," inventor Marc Gleichert, Ser. No. 07/839,602, filing date Feb. 21, 1992, assigned to the same assignee, is incorporated by referenced herein.

The 8B/10B coding of an 8 bit byte of raw data is carried out in two nibbles, a 5 bit nibble and a 3 bit nibble. The 5 bit nibble is encoded to 6 bits and the 3 bit nibble is encoded to 4 bits. The 8B/10B coding is set forth in Table 1 and 2 as given below by Widmer et al.

TABLE 1

5B/6B ENCODING						
NAME	ABCDE	K	D-1	abcdei	D1	abcdei ALTERNATE
D.0	00000	0	+	011000	-	100111
D.1	10000	0	+	100010	-	011101
D.2	01000	0	+	010010	-	101101
D.3	11000	0	d	110001	0	
D.4	00100	0	+	001010	-	110101
D.5	10100	0	d	101001	0	
D.6	01100	0	d	011001	0	
D.7	11100	0	-	111000	0	000111
D.8	00010	0	+	000110	-	111001
D.9	10010	0	d	100101	0	
D.10	01010	0	d	010101	0	
D.11	11010	0	d	110100	0	
D.12	00110	0	d	001101	0	
D.13	10110	0	d	101100	0	
D.14	01110	0	d	011100	0	
D.15	11110	0	+	101000	-	010111
D.16	00001	0	-	011011	+	100100
D.17	10001	0	d	100011	0	
D.18	01001	0	d	010011	0	
D.19	11001	0	d	110010	0	
D.20	00101	0	d	001011	0	
D.21	10101	0	d	101010	0	
D.22	01101	0	d	011010	0	
D/K.23	01101	x	-	111010	+	000101
D.24	00011	0	+	001100	-	110011
D.25	10011	0	d	100110	0	
D.26	01011	0	d	010110	0	
D/K.27	11011	x	-	110110	+	001001
D.28	00111	0	d	001110	0	
K.28	00111	1	-	001111	+	110000
D/K.29	00111	x	-	101110	+	010001
D/K.30	01111	x	-	011110	+	100001
D.31	11111	0	-	101011	+	010100

TABLE 2

3B/4B ENCODING						
NAME	FGH	K	D-1	fghj	D1	fghj ALTERNATE
D/K.x.0	000	x	+	0100	-	1001
D.x.1	100	0	d	1001	0	
D.x.2	010	0	d	0101	0	
D/K.x.3	110	x	-	1100	0	0011
D/K.x.4	001	x	+	0010	-	1101
D.x.5	101	0	d	1010	0	
D.x.6	011	0	d	0110	0	
D.x.P7	111	0	-	1110	+	0001
D/K.y.A7	111	x	-	0111	+	1000
K.28.1	100	1	+	1001	0	0110
K.28.2	010	1	+	0101	0	1010
K.28.5	101	1	+	1010	0	0101
K.28.6	011	1	+	0110	0	1001

Note:

K.x Restricted to K.28

K.y Restricted to K.23, K.27, K.28, K.29, K.30

All the possible 5 bit data values are listed in column "ABCDE" and their corresponding, valid 6 bit 5B/6B codes are listing in the column labeled "abcdei" and in the column labeled "ALTERNATE." If the running disparity has a positive value immediately before the instant that the encoding of the particular raw data is to commence, then, the valid encoded data for that particular byte must be selected from the column of the Table which will not change the RD or will decrease it. From Table 1, since this would correspond to the "+" condition in Column D-1, the only valid code would be in column "abcdei."

The prior art Widmer et al paper describes combinatorial circuits to carry out the above encoding. Accordingly, for codes with disparity +2 and -2, prior 8B/10B encoders provided logic which selected the

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