

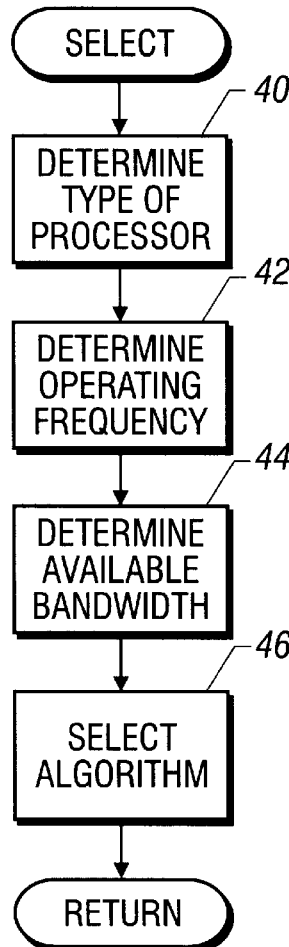


US006122744A

United States Patent [19][11] **Patent Number:** **6,122,744****Rashkovskiy et al.**[45] **Date of Patent:** **Sep. 19, 2000**[54] **SELECTING A ROUTINE BASED ON
PROCESSING POWER**5,862,368 1/1999 Miller et al. 713/501
5,940,607 8/1999 Hwang 713/501[75] Inventors: **Oleg B. Rashkovskiy**, Cupertino;
Ajaya V. Durg, Sunnyvale, both of
Calif.**OTHER PUBLICATIONS**[73] Assignee: **Intel Corporation**, Santa Clara, Calif.Lehoczky et al., "An Optimal Algorithm for Scheduling
Soft-Aperiodic Tasks in Fixed-Priority Preemptive Sys-
tems", IEEE, pp. 110-123, 1992.[21] Appl. No.: **09/082,140**Davis et al., "Scheduling Slack Time in Fixed Priority
Pre-Emptive Systems", IEEE, pp. 222-231, 1993.[22] Filed: **May 20, 1998**Ripoll et al., "An Optimal Algorithm for Scheduling Soft
Aperiodic Tasks in Dynamic-Priority Preemptive Systems",
IEEE, vol. 23, No. 6, pp. 388-400, Jun. 1997.[51] **Int. Cl.**⁷ **G06F 1/04***Primary Examiner*—Glenn A. Auve[52] **U.S. Cl.** **713/300; 713/501***Attorney, Agent, or Firm*—Trop, Pruner & Hu, P.C.[58] **Field of Search** 713/300, 323,
713/501[57] **ABSTRACT**[56] **References Cited****U.S. PATENT DOCUMENTS**

A method includes determining an operating frequency of a
processor. Based on the operating frequency, a routine is
selected from a group of at least two routines, and the
selected routine is executed. The routine may also be
selected based on an unused processing bandwidth that is
available to the processor.

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29 Claims, 4 Drawing Sheets

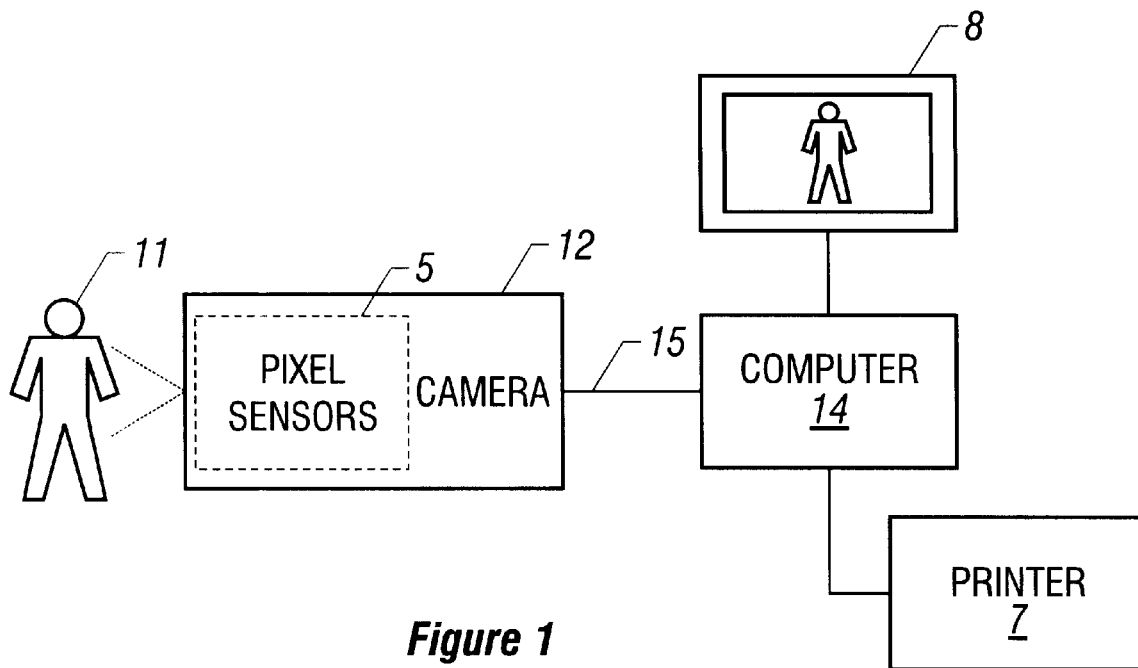


Figure 1
(PRIOR ART)

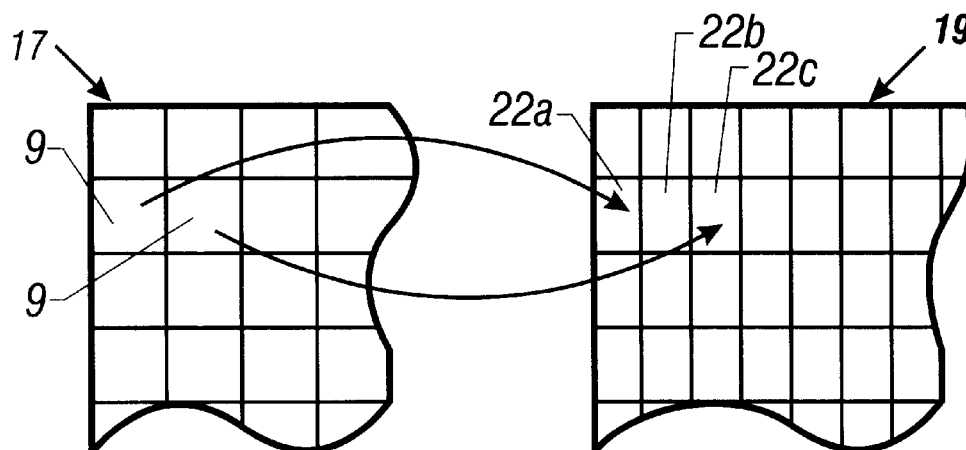
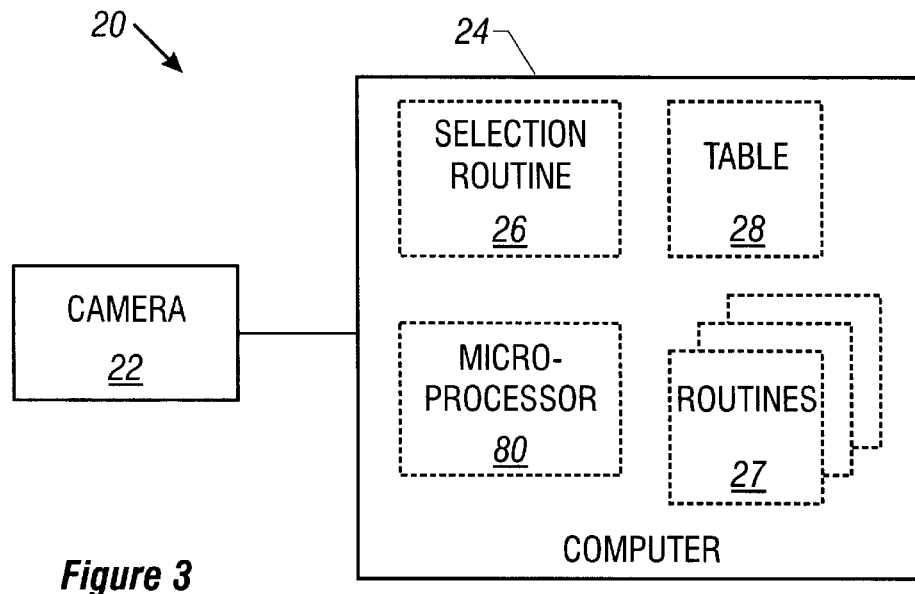
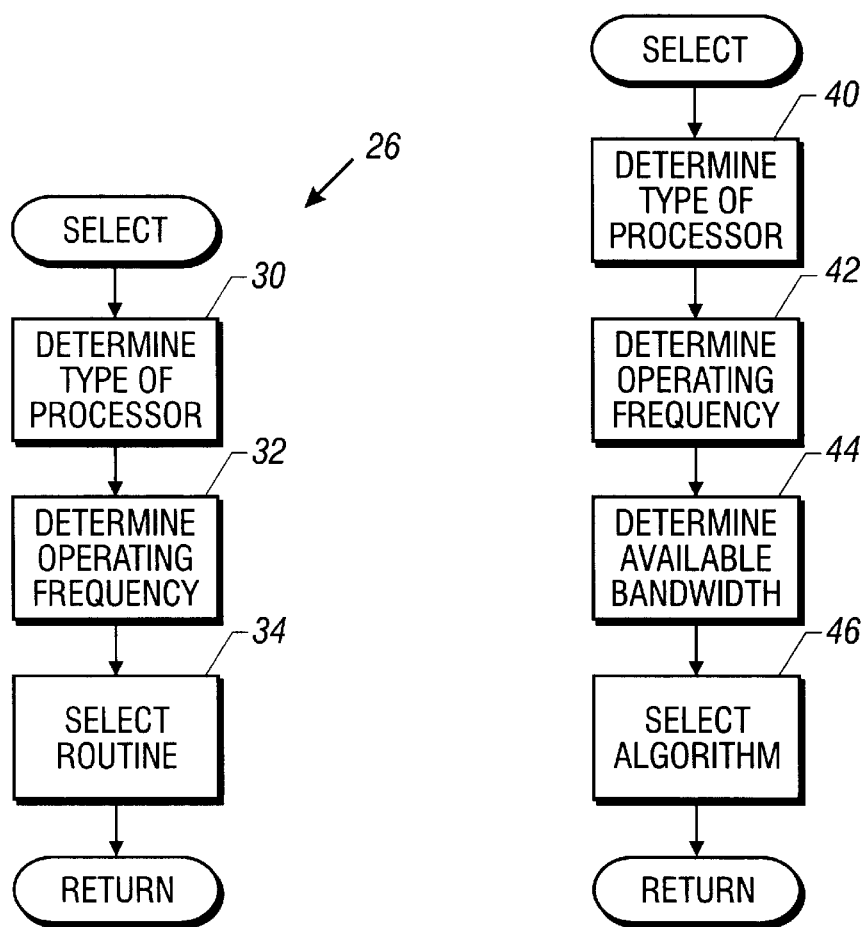


Figure 2
(PRIOR ART)

**Figure 3****Figure 4****Figure 6**

PROCESSOR TYPE	ROUTINE POINTERS				
	RT1	RT1	RT2		RT5
P ₁	RT1	RT1	RT2		RT5
P ₂	RT2	RT3	RT3		RT6
⋮					
P _M	RT4	RT5	RT6		RT8

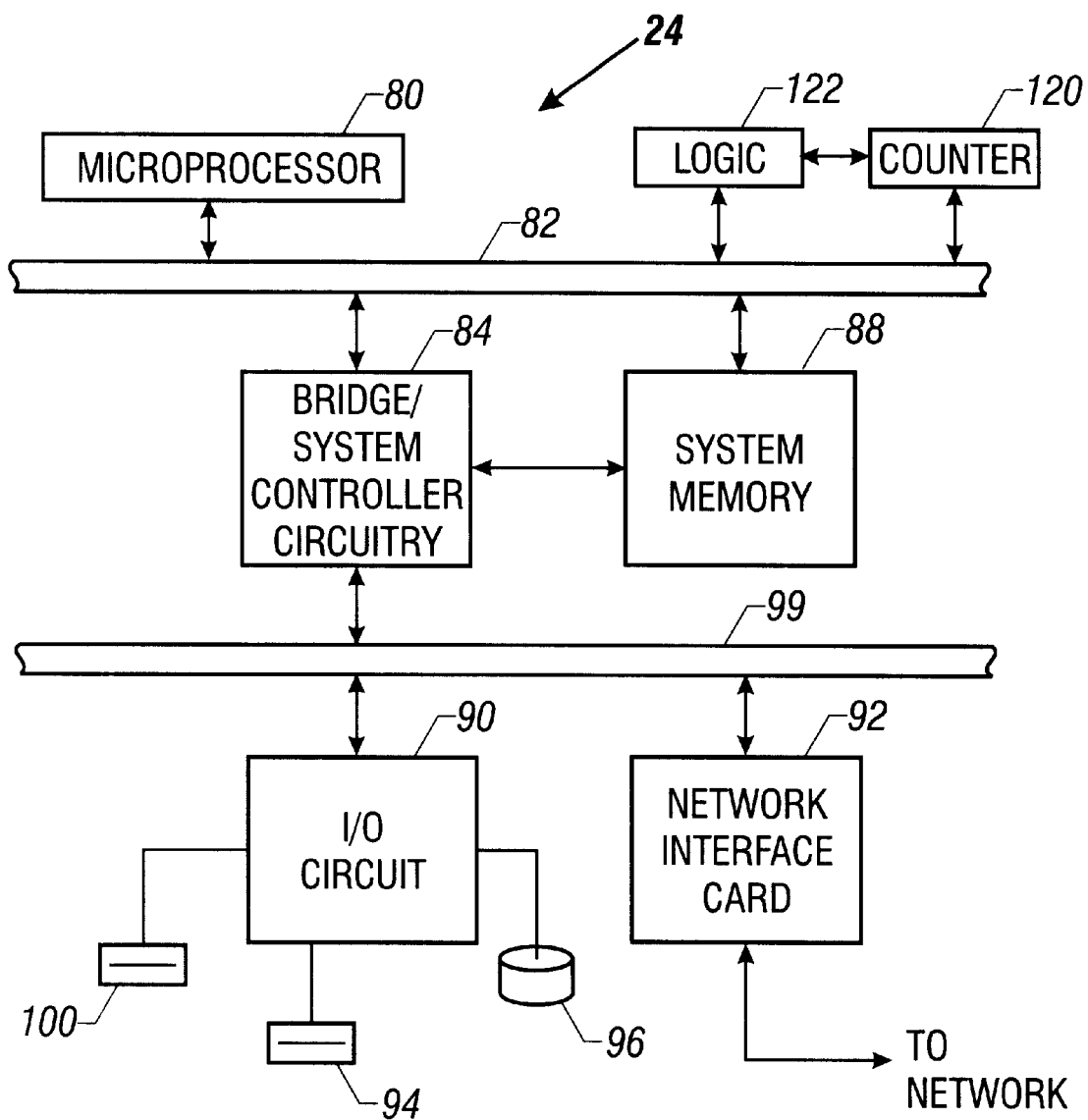
Figure 5

PROCESSOR TYPE	OPERATING FREQUENCY				
	F ₁	F ₂	F ₃	⋯	F _Q
P ₁	PTR1	PTR1	PTR2		PTR5
P ₂	PTR1	PTR1	PTR2		PTR6
⋮					
P _M	PTR4	PTR5	PTR6		PTR8

Figure 7

AVAILABLE BANDWIDTH	ROUTINE POINTERS				
	RT1	RT1	RT2		RT5
B ₁	RT1	RT1	RT2		RT5
B ₂	RT2	RT3	RT3		RT6
⋮					
B _M	RT4	RT5	RT6		RT8

Figure 8

**Figure 9**

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