PHYSICAL PROPERTIES OF RT-LPCVD AND LPCVD POLYSILICON THIN FILMS: APPLICATION TO EMITTER SOLAR CELL.

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ABSTRACT

This investigation was implemented in the framework of a novel all-low thermal budget polysilicon emitter solar cells fabrication technology. A comparative study of structural and electrical properties of thin silicon layer deposited by silane pyrolisis in a classical hot-wall furnace (LPCVD) and a cold-wall RTP reactor (RT-LPCVD) has been made. Deposition conditions and rapid thermal anneals were varied in order to improve the physical properties of RT-LPCVD polysilicon films. The structural properties have been characterized by means of grazing X-ray diffraction and cross-sectional TEM analysis. Sheet resistivity measurements performed on $POCl_3$-doped and subsequently rapid thermal annealed films showed the feasibility of low resistivity films particularly when the polysilicon layers are initially deposited in the amorphous state. Finally, RTCVD polysilicon emitter solar cells with various thicknesses were tested by spectral photo-response analysis.

INTRODUCTION

Polysilicon thin films are widely used in microelectronic technology, especially as contact-emitter in bipolar devices [1]. The interesting physical properties of this material allowed several investigations on polysilicon emitter solar cells [2,3,4]. From this litterature, it appeared that the tight control of polysilicon emitter properties, namely the thickness and the sheet resistance is necessary to avoid front surface recombination and consequently to preserve long minority carrier lifetimes.

Up to date, polysilicon films used in these structures are realized in conventional hot-wall furnaces (CFP) by combination of low temperature processes including LPCVD with in-situ doping followed by a drive-in thermal treatment [2,5]. It is well-known that the latter process produces a relatively high contact sheet resistance due to incomplete electrical activation. So, low thermal budget-Rapid Thermal Annealing (RTA) seems to be a potential alternative way guaranteeing at one, sufficient electrical activation and at the same time suppressing undesirable dopant profile broadening. Furthermore, it is clearly established that the polysilicon/silicon substrate interface control constitutes the key parameter for poly-emitter device performance. Indeed, the presence of a good quality ultra-thin interfacial oxide allows to reduce back-injection current and also to increase the open circuit voltage, Voc [4]. For this purpose, thermally grown oxide is often chosen owing to its thermal stability with respect to native or chemical oxide. However, the oxidation kinetics must be greatly reduced as the interfacial oxide layer must be carrefully kept in the 1-3 nm thickness range [6]. This condition can be partly satisfied by using Rapid Thermal Oxidation in O_2 [7] or N_2O ambient [8]. Besides, in order to protect the oxide layer from any external contamination, one may suggest to insert the polysilicon LPCVD sequence in the same reactor without handling of the wafer. This deposition technique is commonly called Rapid Thermal LPCVD (RT-LPCVD) [9]. Therefore, taking into account all these above-mentioned process steps, we may suggest a novel approach of an all-low thermal budget poly-emitter solar cells technology. This attractive concept was already introduced in microelectronic technologies (MOS, BiCMOS,...) and is familiarly called: integrated Rapid Thermal Multiprocessing (RTMP) [10].

In the present paper, we attempt to estimate separately each of the different steps in order to demonstrate the feasibility of such solar-cell devices fabrication. Polysilicon films deposition was studied as a function of process parameters (pressure, temperature). Structural and electrical polysilicon films properties were respectively characterized by X-Ray Diffraction (XRD), Transmission Electron Microscopy (TEM) and four-point probe sheet resistivity measurements. Finally, photo-responses of RT-LPCVD polysilicon emitter solar-cells are also given.

EXPERIMENTAL DETAILS

Two different types of substrates (P: 1 Ω.cm) were used according to whether films have been directly formed on virgin 2-in. (111) Cz-grown Si wafers (series # 1) or on the same substrates initially covered with 100 nm of thermally grown SiO_2 (series # 2). RTP treatments were carried out in a Jipelec™ cold-wall reactor. This machine is a non load-locked system which consists on a cylindrical stainless steel chamber designed to process wafers up to 4 in. diameter. Wafer front-heating is made through a quartz window by means of a single bank of

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First WCPEC; Dec. 5–9, 1994; Hawaii

12 W-halogen lamps allowing to reach heating rates of few 100 °C/s. Temperature is monitored with an optical pyrometer viewing the wafer underside. This pyrometer is periodically K-thermocouple calibrated. A base pressure in the 10^{-4}- 10^{-5} mbar range can be achieved in few minutes by using a combination of rotary and turbomolecular pumps insuring a fast turnaround process. RT-LPCVD polysilicon layers were prepared by silane pyrolisis using a SiH4/Ar mixture (10%) at fixed flow rate (50-100 sccm) and process pressure ranging from 1 mbar to 5 mbar. After this, the samples were POCl3 doped at 850°C for 15 minutes.

On the other hand, comparative LPCVD polysilicon films (450 nm) were elsewhere formed in a conventional furnace at 670°C from N2-diluted silane/phosphine mixture (250/1) and a total pressure of 1 Torr.

Both types of samples were subsequently submitted respectively to a dry oxidation at 800°C/10min and a drive-in RTA under atmospheric N2 ambient for 20s at various temperatures (950 °C, 1000°C, 1050 °C).

Polysilicon film thicknesses have been determined by mechanical profilometry after an appropriate chemical etching. Resistivity measurements were made by using the conventional four-point probe technique. Further details on the overall deposition operation and analysis procedures are described elsewhere [11].

RESULTS AND DISCUSSION

Deposition rates

The deposition kinetics of polysilicon films were studied for the series 2 at a process pressure of 1 mbar. An Arrhenius plot of the deposition rates versus the deposition temperature is shown in figure 1. The two usual deposition regimes are observed with a transition temperature at 750°C. This temperature emphasizes a particular advantage of cold wall reactors which allow to achieve deposition rates up to 200 nm/min in the reaction limited regime wherein thickness homogeneity over large diameter wafers is mostly thermally controlled. Indeed, cold-walled systems limit parasitic gas-phase nucleation commonly observed at relatively lower temperatures (620°C-650°C) in classical hot wall furnaces[12]. Besides, an activation energy corresponding to the silane chemistry (1.7eV) is obtained in the surface reaction limited regime. This typical value has been reported by others [13] for polysilicon RT-LPCVD and well agrees with LPCVD results. Above 750°C, the deposition becomes less dependent on the wafer temperature, as it is mainly controlled by the diffusional transfer of reactant molecules through the boundary layer at the wafer surface.

Furthermore, thin oxide films were achieved taking into account the growth kinetics results obtained in our group by using a stagnant ambient of O_2 or N_2O with a 0.15 bar overpressure and a process temperature fixed in the 1000 °C-1200 °C [14]. From this study, it is noteworthy that the growth rate is greatly enhanced at the initial stage of Si oxidation. This fact is usually ascribed to a faster diffusion of oxidizing species through the very thin oxide layer. So, as suggested by Kermani et al. [6], it appears preferable in the future to work at a lower oxidation temperature and/or oxygen process pressure. Nevertheless, we have evidenced among others the ability of our system to achieve reproducible in-situ oxide/polysilicon stack with acceptable MOS device performance [15].

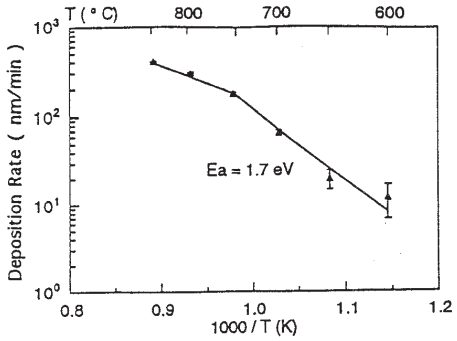

Figure 1: RT-LPCVD deposition rates as a function of the deposition temperature. 1 mbar, 10 % SiH4 in Ar, 100 sccm.

Structural properties

In previous works, we have shown that amorphous to crystalline temperature transition occurs at above 650°C [16]. This relatively higher value with respect to LPCVD films (580°C-600°C) denotes a retarded crystallization likely due to the residual water vapor which limits the vacant sites surface density and consequently slows down the reactive species diffusion. This discrepancy is probably linked to the way by which deposition is started. Gas-switching in classical furnaces allows previous thermal desorption of both substrates and internal wall whereas temperature-switching in RTP reactors does not.

In addition, both XRD analysis and electron-diffraction patterns (TEM) have shown the appearance of a dominant <111> grain orientation instead of the <220> one as usually reported for LPCVD polysilicon layers [12]. In general, <111> texture depicts a solid phase crystallization of initially amorphous deposited layer. Between 650 °C and 750 °C, we expected that the RT-LPCVD polysilicon films are partially crystalline (mixte) with a reduced degree of amorphicity as the deposition temperature increases. Above 750 °C, the films appears to be totally crystallized and exhibits a columnar-like structure along the whole film thickness as illustrated by X-TEM observations presented in ref. [11].

The deposition durations were chosen according to needed poly-emitter thicknesses which must be within the 70-150 nm range, in order to improve the photocurrent by reducing the carrier recombination [2, 4]. At 600 °C, e.g., a deposition time of at least 10 min is necessary to achieve the thickness bottom limit. As shown in figure 2, an incubation time of approximately 12-13 s is found by intersection of a least-squares-fitted line corresponding to the film thickness variation vs. the deposition duration at 750 °C on small-area control specimens (2 x 2 cm^2) [11].

This incubation time could be higher at lower

deposition temperatures [17]. In this case, one may expect that the effective deposition time might be smaller than the crystallization time, i.e., the needed time for the layer to be completely crystalline.

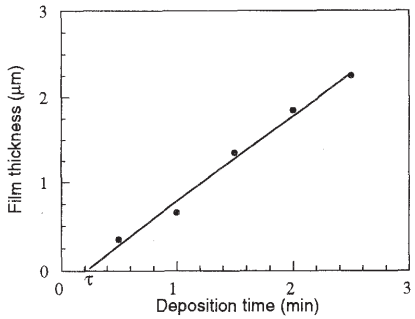

Figure 2: Polysilicon films thickness vs. deposition time. 750 ° C, 5 mbar, 10 % SiH4 in Ar, 50 sccm.

Sheet resistance

On table 1 are listed the sheet resistance results corresponding to the POCl3-doped samples (series # 2) before (BA) and after (A) the RTA treatment. After the predeposition step, a typical phosphorus concentration of about $2x10^{20}$ cm^{-3} uniformly distributed along the film thickness has been measured [18]. It can be noted that the sheet resistance is significantly reduced (30-40 %) after annealing step (1050 °C/20 s), except for the specimen deposited at 750 °C.

Table 1: Sheet resistance of RTCVD polysilicon films deposited at 5 mbar in the 650 °C-850 °C temperature range: (BA) before and (A) after RTA annealing (1050°C/20s). a: amorphous; c: crystalline.

Deposition température (°C)	Thickness (nm)	Sheet resistance (Ω/sq) (BA)	(A)	initial structure
650	90	139	85	a
700	160	93	59.3	a+c
750	95	353	305	c
800	135	123	—	c
850	160	74	55.5	c

The influence of the RTA temperature on the sheet resistance of the emitter layer (series # 1) is summarized on table 2 both for in situ-doped LPCVD polysilicon films and POCl3-doped RT-LPCVD amorphous silicon films deposited at 600 °C. Noting that a chemical phosphorus concentration of around 10^{19} cm^{-3} have been determined by ion-probe analysis for the LPCVD layers. In both cases, the main feature is that the sheet resistance decreases by a factor 2-3 when the anneal temperature is varied between 950 °C to 1050 °C.

Table 2: Effect of RTA treatment at fixed duration (20s) on the sheet resistance of LPCVD (450 nm) and RT-LPCVD polysilicon films (80 nm, 120 nm).

RTA (°C)	Sheet resistance (Ω/sq) poly-Si LPCVD (450 nm)	a-Si RT-LPCVD (80 nm)	a-Si RT-LPCVD (120nm)
none	200	35	13.4
950	84	21	8.7
1000	73	—	–
1050	44	6.7	7

Besides, we can see that the lowest sheet resistance is obtained for the crystallized amorphous material suggestive to a relatively more important grain growth under RTA treatment. But this grain growth is likely limited by the film thickness. Furthermore, it is worth noting that the sheet resistance is lowered when the RT-LPCVD films are directly deposited on the virgin silicon substrate (see tables 1 and 2), and even more at higher RTA temperature. This indicates that further dopant loss by diffusion through interfacial oxide into the substrate has occured [19].

Spectral response of solar cells

Taking into account the sheet resistance results cited in the above section, we have selected thin silicon films deposited in the amorphous phase on non textured single crystal silicon.

Spectral photo-response measurements of unannealed poly- emitter silicon solar cells with various thicknesses (80nm, 120 nm and 160 nm) are shown in Fig. 3. Front and back contacts were set up by screen printing either with the so-called N ink for the front contact, or with a P ink for the back contact.

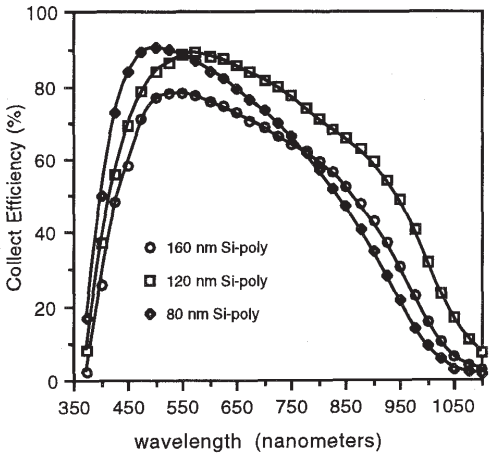

Figure 3: spectral photoresponses of unannealed RT-LPCVD poly-emitter silicon solar cells.

As expected, the ultraviolet and blue responses of the polysilicon emitter devices are improved when the emitter thickness is decreased. On the other hand, it can be noted that the infrared photoresponse loss is obviously due to the non optimized substrates used in this prospective study. In addition, some attempts on RTA annealed samples (1050 °C/20 s) have shown a device structure degradation revealed by a photo-response lowering which might be also linked to the substrate quality (leakage current, minority carrier diffusion length reduction).

Finally, we can conclude that optimization of the efficiency of a polysilicon emitter requires that a compromise be made between the loss of blue response encountered with series resistance associated with a thin layer [4].

SUMMARY

This work was devoted to the comparative study of the structural and electrical properties of thin silicon films deposited by RT-LPCVD with respect to conventional LPCVD films. We have introduced the new concept of Rapid Thermal Multiprocessing (RTMP) in the poly-emitter silicon solar cells technology. This particular technique offers a convenient means for all-low thermal budget integrated processing in order to achieve in-situ compatible sequences like as cleaning, deposition or growth of multiple layers and heat treatments. Electrical measurements showed that the lowest sheet resistance is achieved for the crystallized amorphous material owing to the grain growth enhancement under RTA treatment and even more when the films are directly formed on virgin silicon substrates.

Furthermore, it appeared that the blue response is improved as the poly-emitter thickness decreases. Other photoresponse measurements are needed and preferably on adequate Float-Zone substrates.

AKNOWLEDGMENTS

This work was supported by CNRS-ECOTECH and AFME, with the collaboration of Photowatt International S.A. 38300, Bourgoin-Jallieu, France.

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