

# EXHIBIT A

(12) **United States Patent**  
**Hall et al.**

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(45) **Date of Patent:** **Nov. 1, 2011**

(54) **DEVICE FOR AVOIDING PARASITIC CAPACITANCE IN AN INTEGRATED CIRCUIT PACKAGE**

(75) Inventors: **Jeffrey Hall**, San Jose, CA (US); **Shawn Nikoukary**, Santa Clara, CA (US); **Amar Amin**, Milpitas, CA (US); **Michael Jenkins**, San Jose, CA (US)

(73) Assignee: **LSI Corporation**, Milpitas, CA (US)

(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 365 days.

(21) Appl. No.: **11/277,188**

(22) Filed: **Mar. 22, 2006**

(65) **Prior Publication Data**  
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(51) **Int. Cl.**  
**H01L 23/48** (2006.01)

(52) **U.S. Cl.** ..... **257/777; 257/E23.019; 257/E23.151; 257/758**

(58) **Field of Classification Search** ..... **257/792, 257/777, 700, 798, 728, E23.019, E23.151, 257/E23.152, E23.153, E23.175, 758, 693, 257/698, 760, 691, 692, E23.062, 778**  
See application file for complete search history.

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*Primary Examiner* — Wael Fahmy

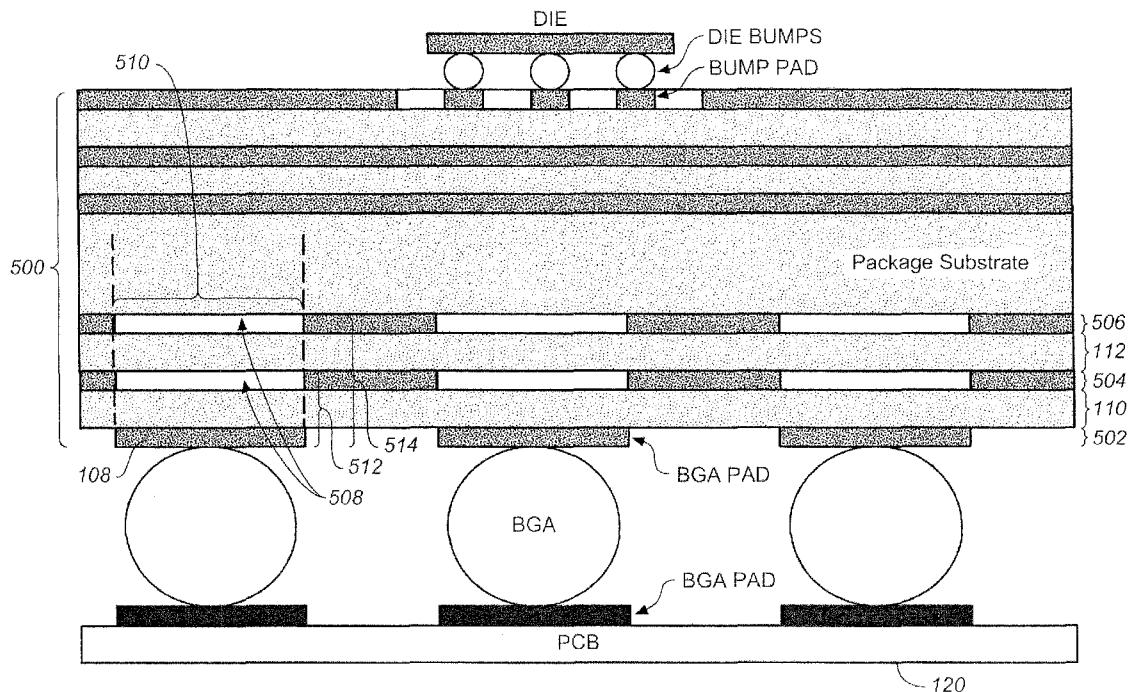
*Assistant Examiner* — Sarah Salerno

(74) *Attorney, Agent, or Firm* — Otterstedt, Ellenbogen & Kammer, LLP

(57) **ABSTRACT**

An integrated circuit package substrate includes a first and an additional electrically conductive layer separated from each other by an electrically insulating layer, a contact pad formed in the first electrically conductive layer for making a direct connection between the integrated circuit package substrate and a printed circuit board, and a cutout formed in the additional electrically conductive layer wherein the cutout encloses an area that completely surrounds the contact pad for avoiding parasitic capacitance between the additional electrically conductive layer and the printed circuit board.

**19 Claims, 6 Drawing Sheets**



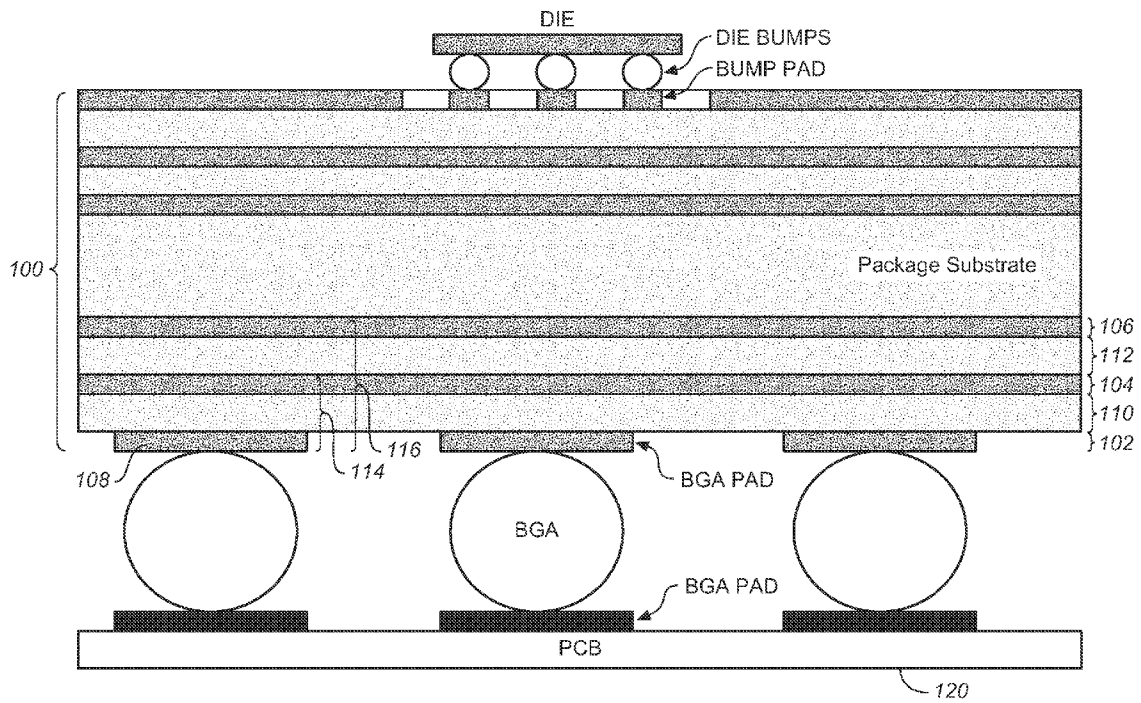


FIG. 1 (PRIOR ART)

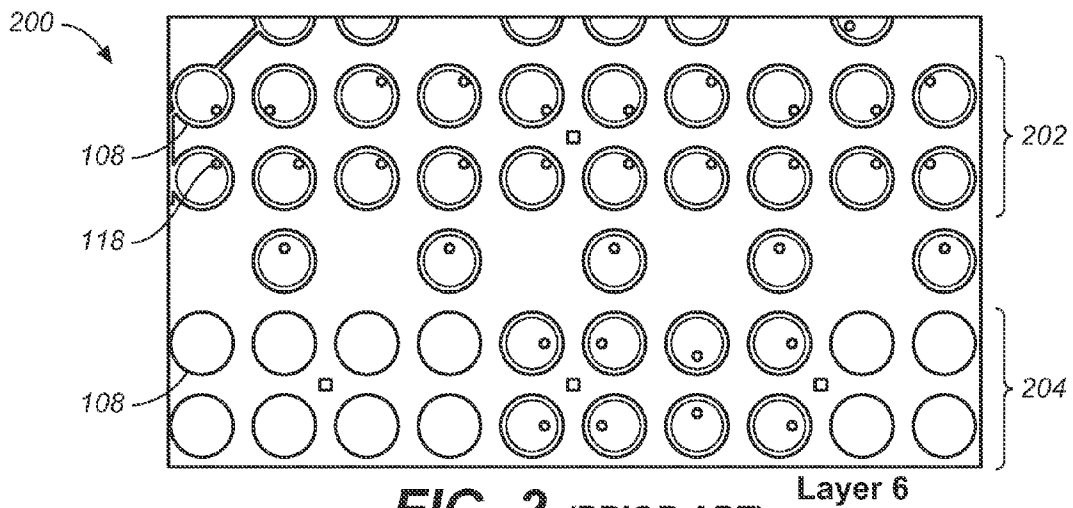


FIG. 2 (PRIOR ART)

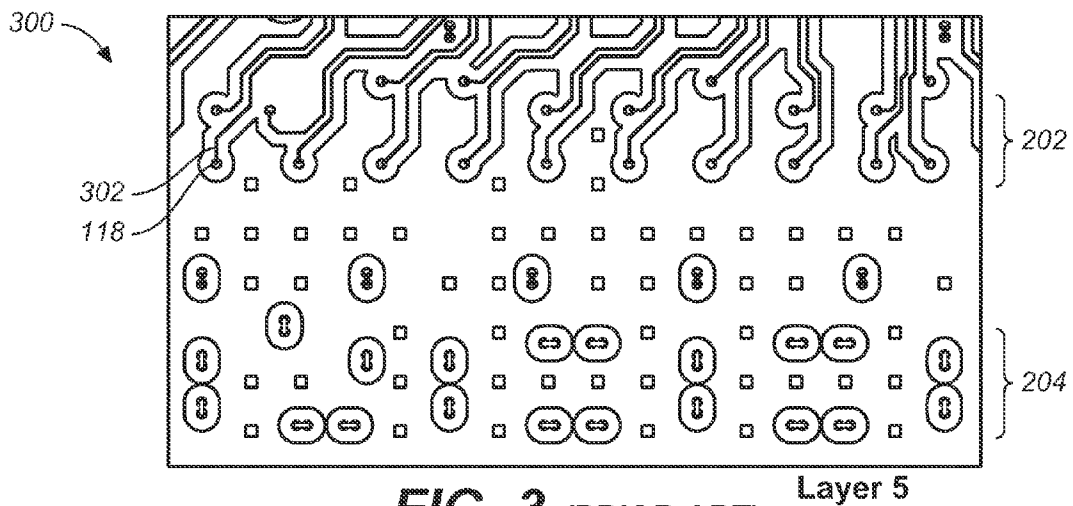


FIG. 3 (PRIOR ART)

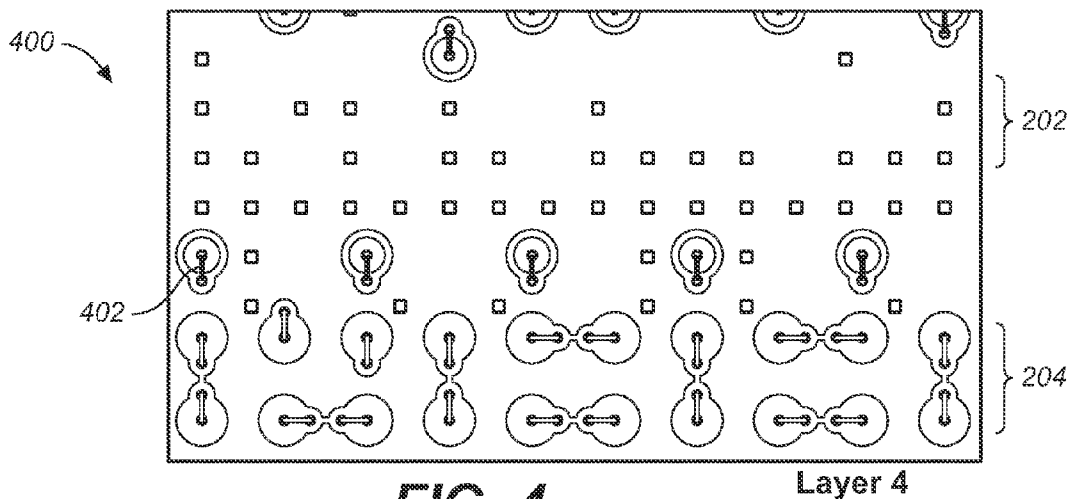


FIG. 4 (PRIOR ART)

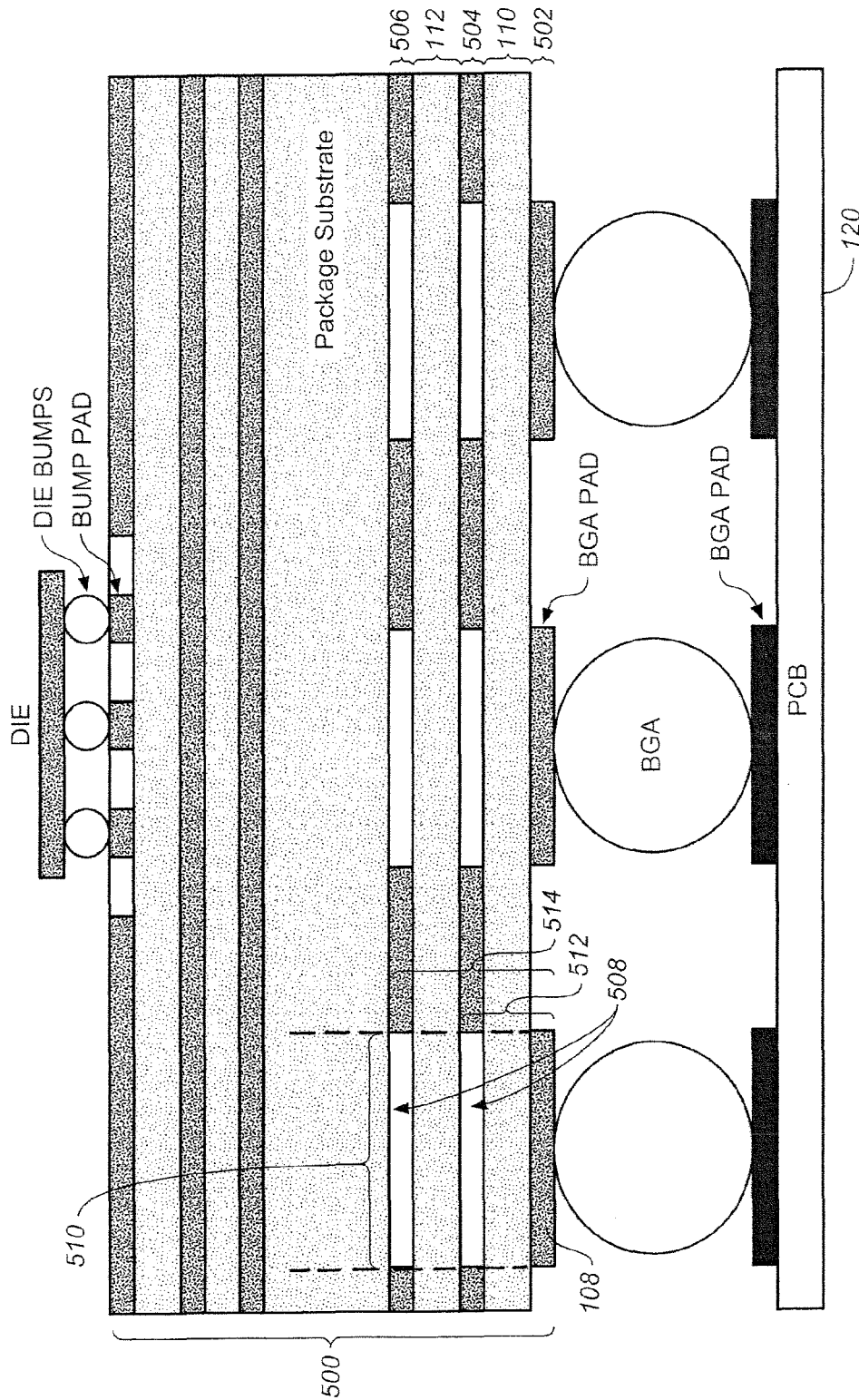


FIG. 5

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