

# EXHIBIT B

(12) **United States Patent**  
**Hall et al.**

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(45) **Date of Patent:** **Oct. 16, 2012**

(54) **METHODS FOR AVOIDING PARASITIC CAPACITANCE IN AN INTEGRATED CIRCUIT PACKAGE**

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(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/252,632**

(22) Filed: **Oct. 4, 2011**

(65) **Prior Publication Data**  
 US 2012/0021599 A1 Jan. 26, 2012

**Related U.S. Application Data**  
 (62) Division of application No. 11/277,188, filed on Mar. 22, 2006, now Pat. No. 8,049,340.

(51) **Int. Cl.**  
**H01L 21/4763** (2006.01)  
 (52) **U.S. Cl.** ..... **438/622; 257/758; 257/E21.536**  
 (58) **Field of Classification Search** ..... None  
 See application file for complete search history.

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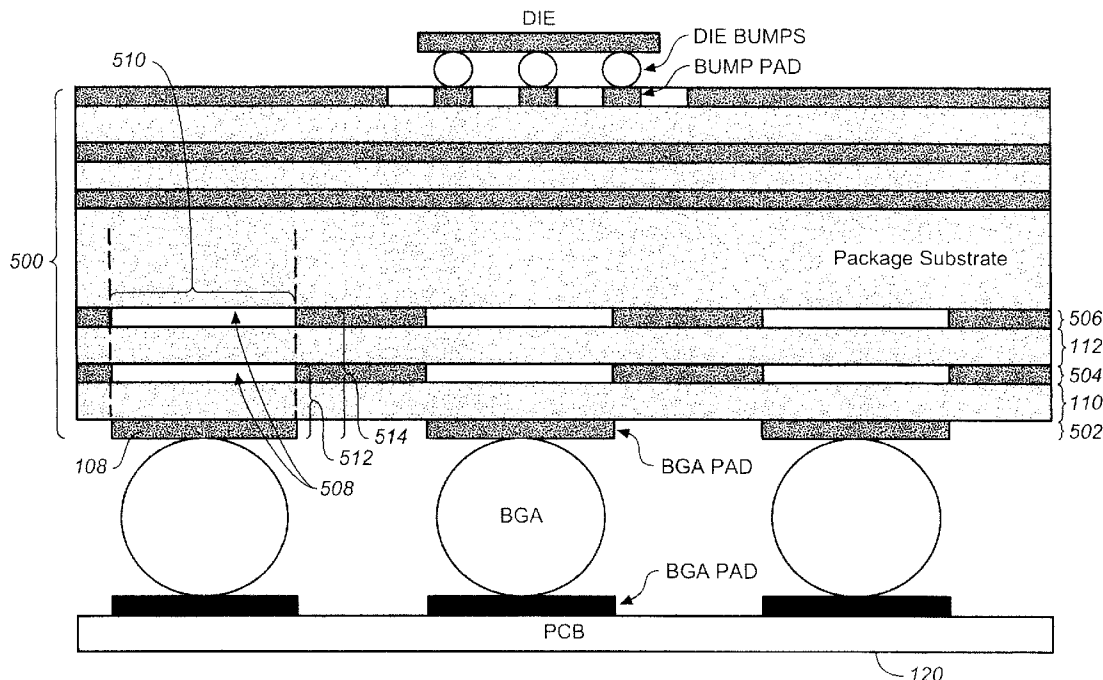
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(57) **ABSTRACT**

An integrated circuit package substrate includes a first and an additional electrically conductive layer separated from each other by an electrically insulating layer, a contact pad formed in the first electrically conductive layer for making a direct connection between the integrated circuit package substrate and a printed circuit board, and a cutout formed in the additional electrically conductive layer wherein the cutout encloses an area that completely surrounds the contact pad for avoiding parasitic capacitance between the additional electrically conductive layer and the printed circuit board.

**20 Claims, 6 Drawing Sheets**



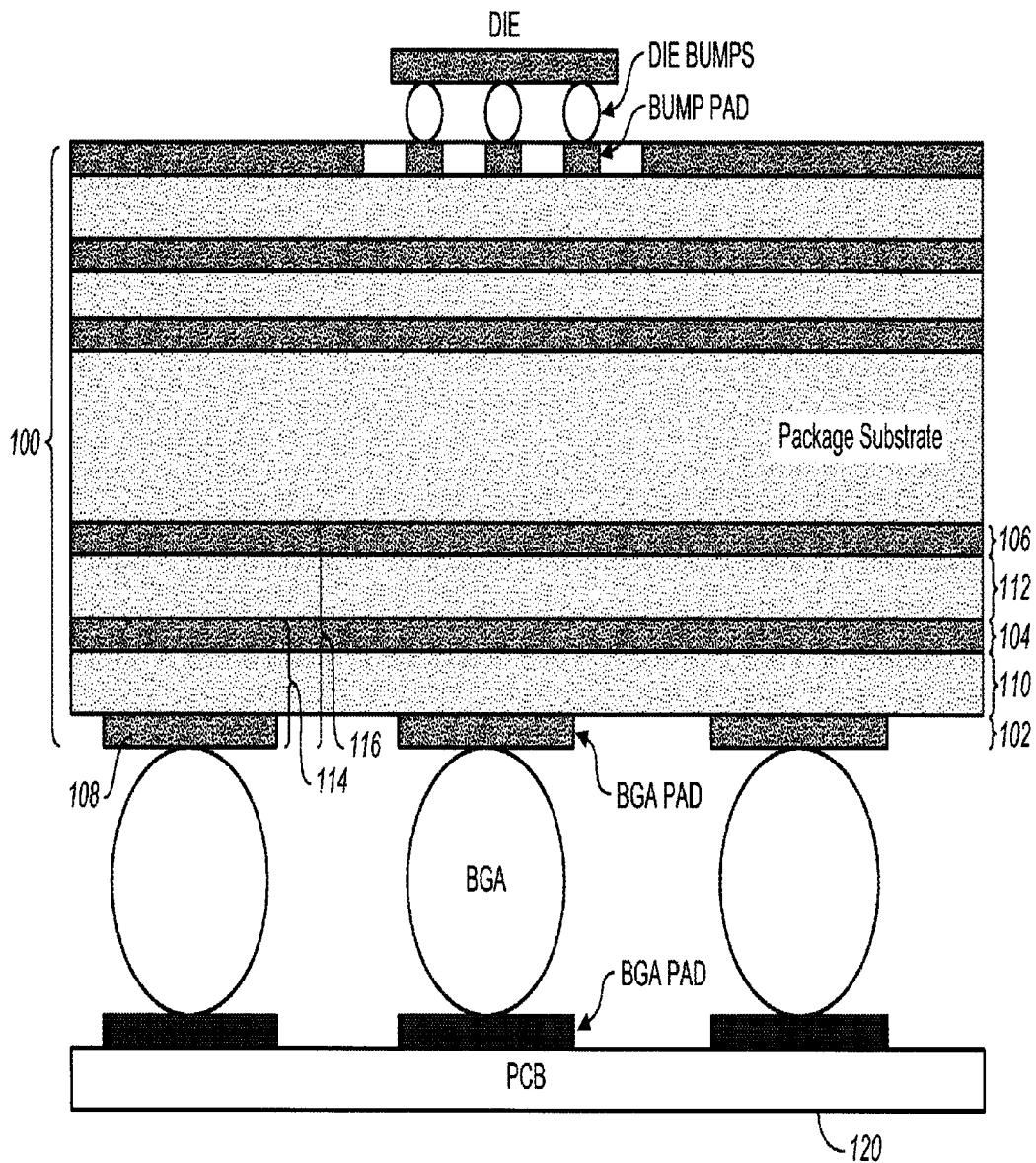


FIG. 1 (PRIOR ART)

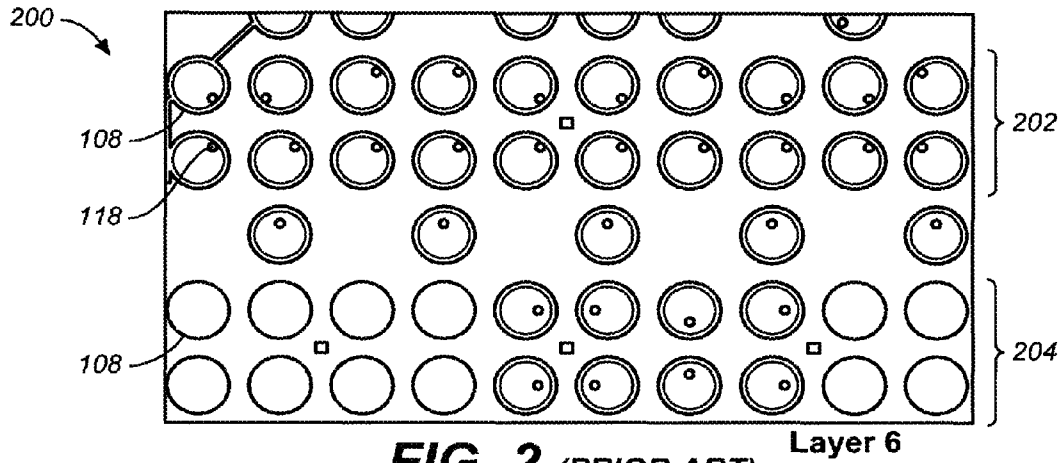


FIG. 2 (PRIOR ART)

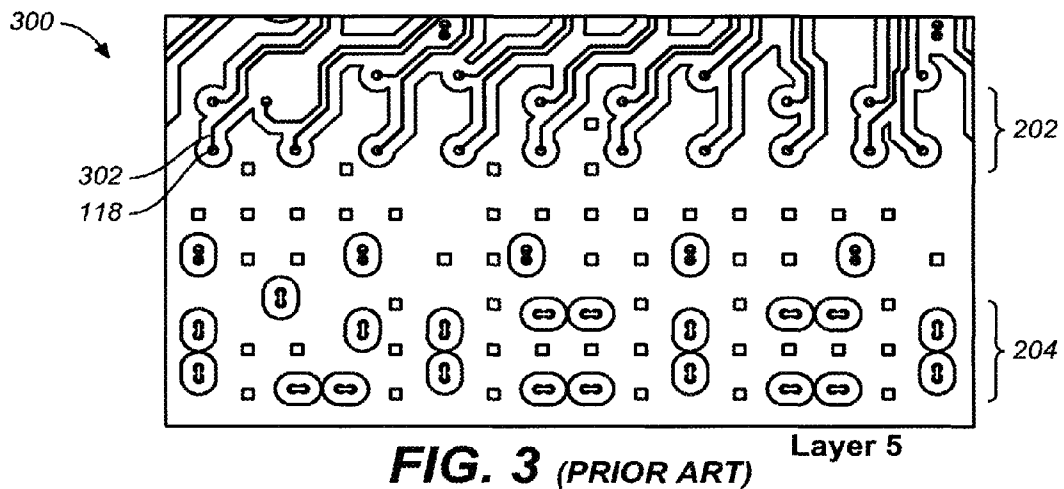


FIG. 3 (PRIOR ART)

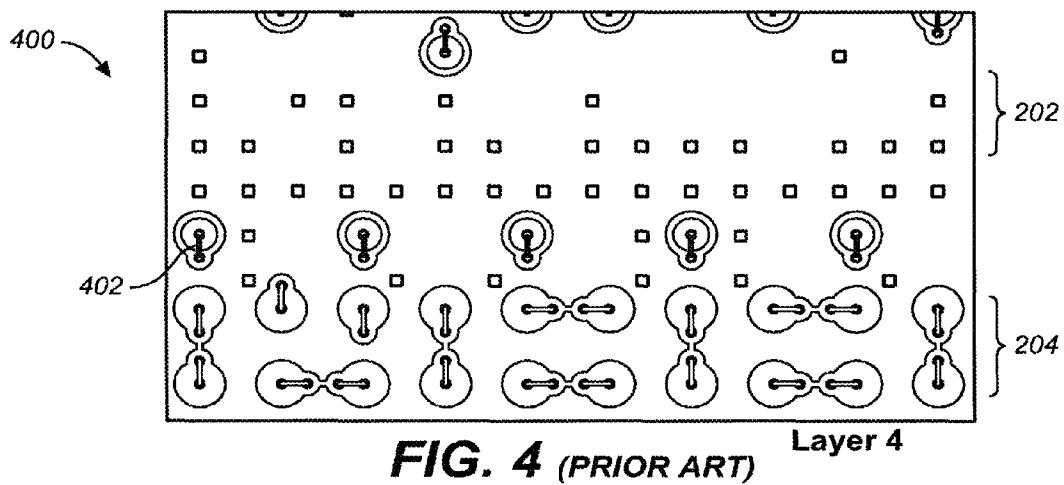


FIG. 4 (PRIOR ART)

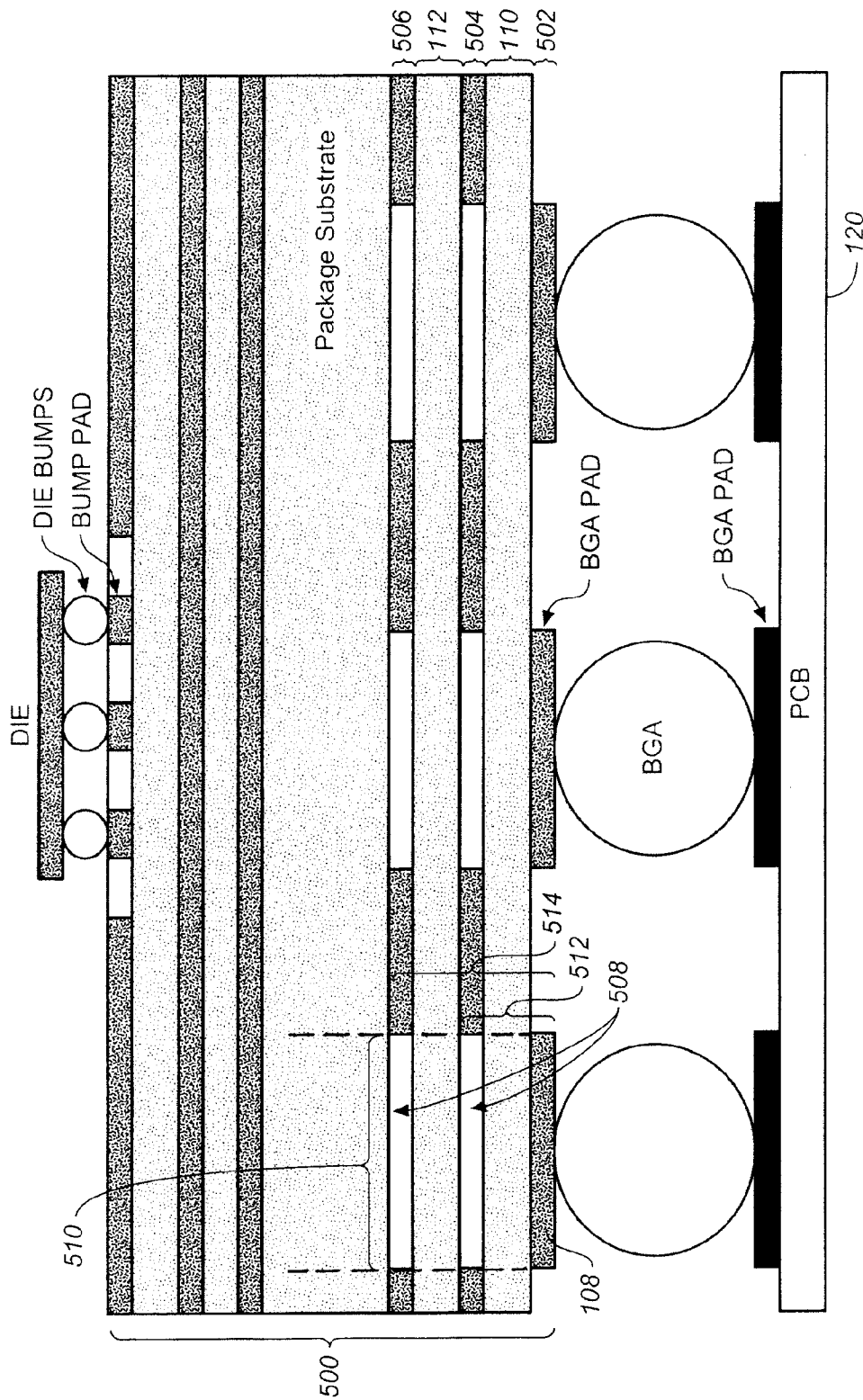


FIG. 5

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