

EXHIBIT E

(12) **United States Patent**
Easter et al.

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(45) **Date of Patent:** **Jul. 22, 2003**

(54) **METHOD FOR CHEMICAL/MECHANICAL PLANARIZATION OF A SEMICONDUCTOR WAFER HAVING DISSIMILAR METAL PATTERN DENSITIES**

(75) Inventors: **William G. Easter**, Orlando, FL (US);
Sudhanshu Misra, Orlando, FL (US);
Vivek Saxena, Orlando, FL (US)

(73) Assignee: **Agere Systems Inc.**, Allentown, PA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/415,529**

(22) Filed: **Oct. 8, 1999**

(51) **Int. Cl.**⁷ **H01L 21/302**

(52) **U.S. Cl.** **438/692**; 438/626; 438/633;
438/699

(58) **Field of Search** 438/626, 631-634,
438/645, 692

(56) **References Cited**

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Primary Examiner—Wael Fahmy
Assistant Examiner—Marcos D. Pizarro-Crespo

(57) **ABSTRACT**

The present invention provides a method of manufacturing an integrated circuit including planarizing a semiconductor wafer surface. In one embodiment, the method comprises forming a dielectric layer over a first level having an irregular topography, depositing a sacrificial material over the dielectric layer, and then planarizing the semiconductor wafer surface to a planar surface. More specifically, the dielectric layer forms such that it substantially conforms to the irregular topography of the first level. The sacrificial material is formed to a substantially planar surface over the dielectric layer. Thus, the sacrificial material provides a substantially uniform chemical/mechanical planarization (CMP) process removal rate across the semiconductor wafer surface. In the ensuing step, planarizing the semiconductor wafer surface to a planar surface removes the sacrificial material and a portion of the dielectric layer with a CMP process.

14 Claims, 4 Drawing Sheets

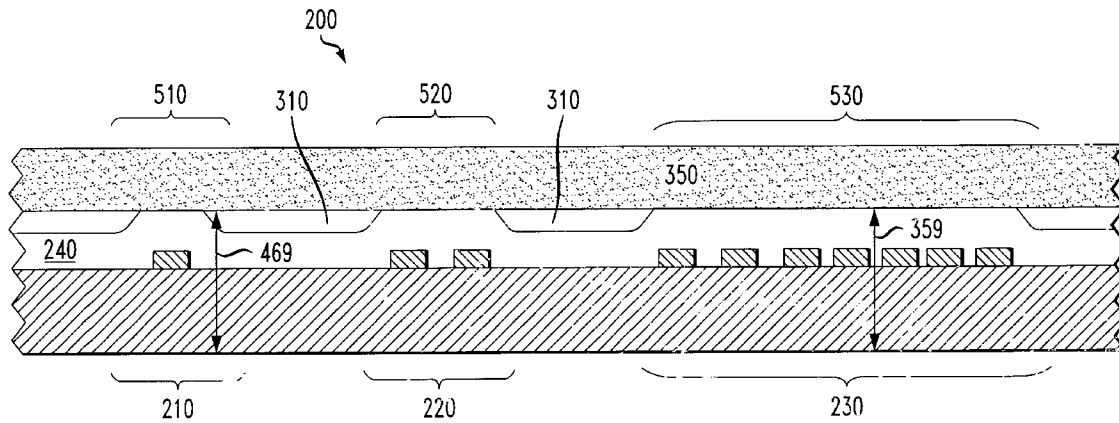


FIG. 1A

PRIOR ART

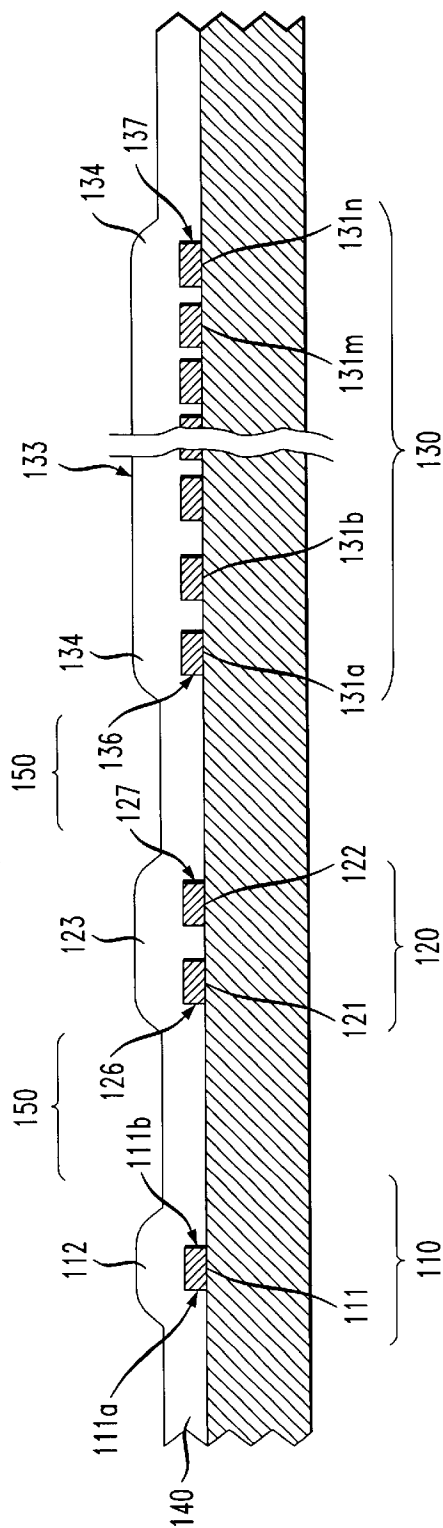


FIG. 1B

PRIOR ART

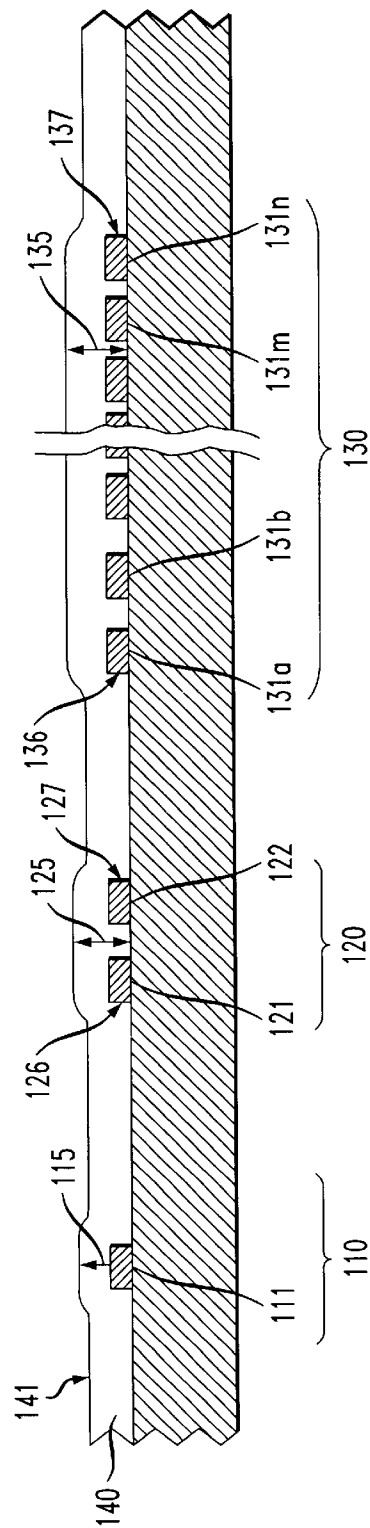


FIG. 2

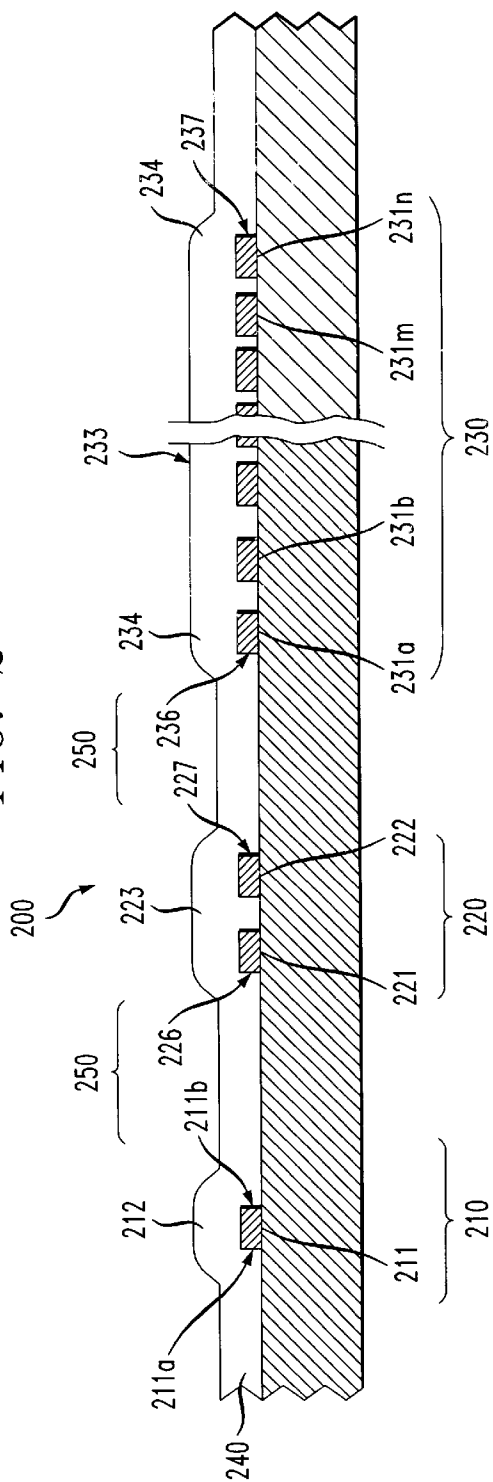


FIG. 3

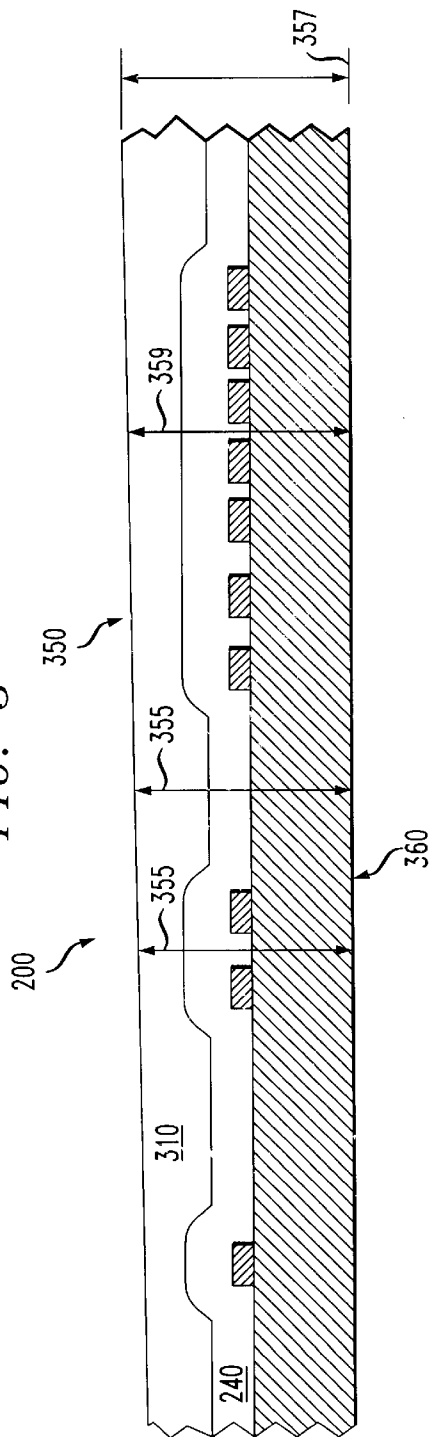


FIG. 4

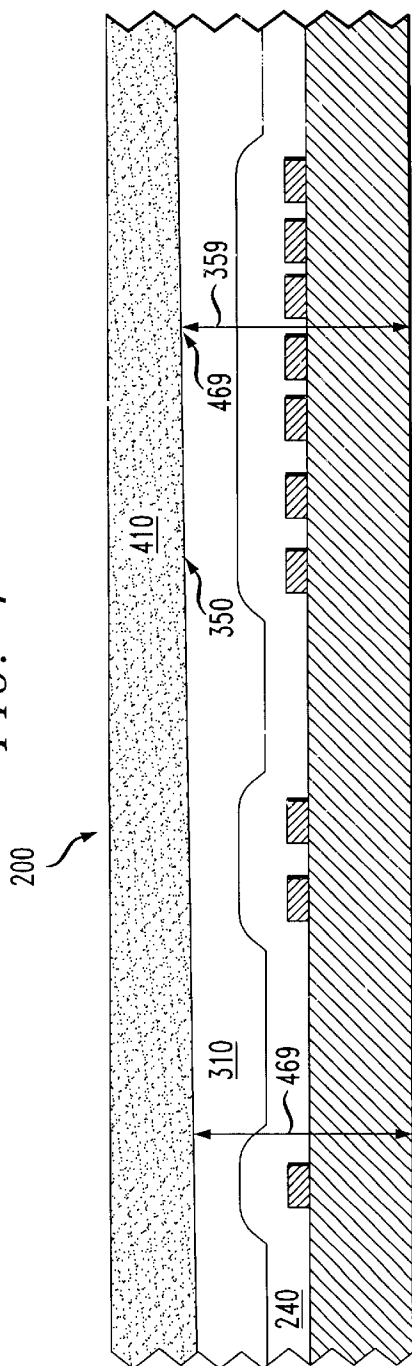
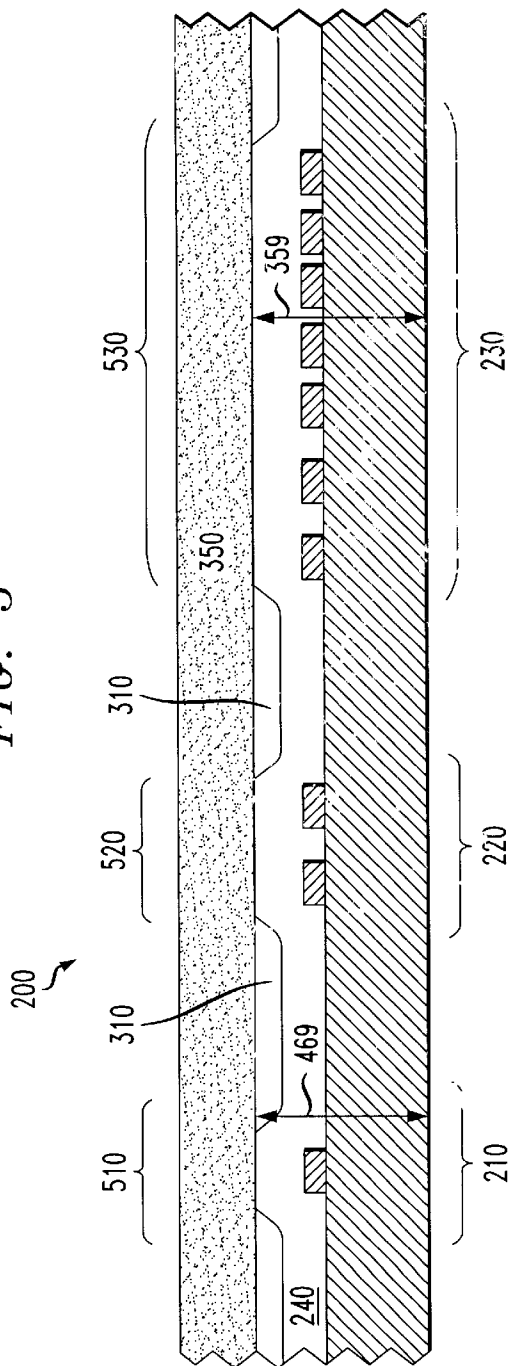


FIG. 5



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