

# EXHIBIT G

(12) **United States Patent**  
**Banerjee et al.**

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(54) **HIGH PERFORMANCE SI-GE DEVICE  
MODULE WITH CMOS TECHNOLOGY**

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\* cited by examiner

(75) Inventors: **Robi Banerjee**, Gresham, OR (US);  
**Derryl J. Allman**, Camas, WA (US);  
**David T. Price**, Gresham, OR (US)

*Primary Examiner*—David Nelms

*Assistant Examiner*—Tu-Tu Ho

(74) *Attorney, Agent, or Firm*—Trexler, Bushnell,  
Giangiori, Blackstone & Marr, Ltd.

(73) Assignee: **LSI Logic Corporation**, Milpitas, CA  
(US)

(57) **ABSTRACT**

(\* ) Notice: Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 0 days.

A semiconductor device wherein some parts of a circuit are  
disposed on Si—Ge regions and others are implemented in  
Silicon substrate regions of the chip. The Si—Ge region  
provides that carrier flow is forced to the surface channel  
region which helps reduce short channel effects. A method  
of making such a semiconductor device is also provided and  
includes steps of forming a thermal oxide layer on a Silicon  
substrate, masking at least a portion of the thermal oxide  
layer in order to expose a portion of the Silicon substrate,  
epitaxially growing an Si—Ge layer on the exposed portion of  
the Silicon substrate, epitaxially growing a Silicon layer on  
the Si—Ge layer, and continuing manufacture of the device  
by forming a circuit on the Si—Ge regions and non-Si—Ge  
regions of the semiconductor device.

(21) Appl. No.: **10/288,410**

(22) Filed: **Nov. 5, 2002**

(51) **Int. Cl.**<sup>7</sup> ..... **H01L 31/117**

(52) **U.S. Cl.** ..... **257/616; 257/18; 257/19**

(58) **Field of Search** ..... **257/616, 18, 19**

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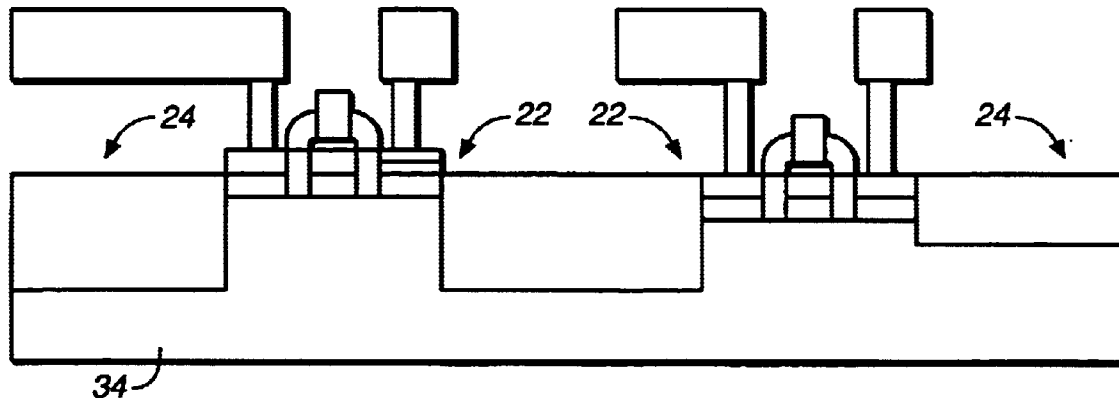
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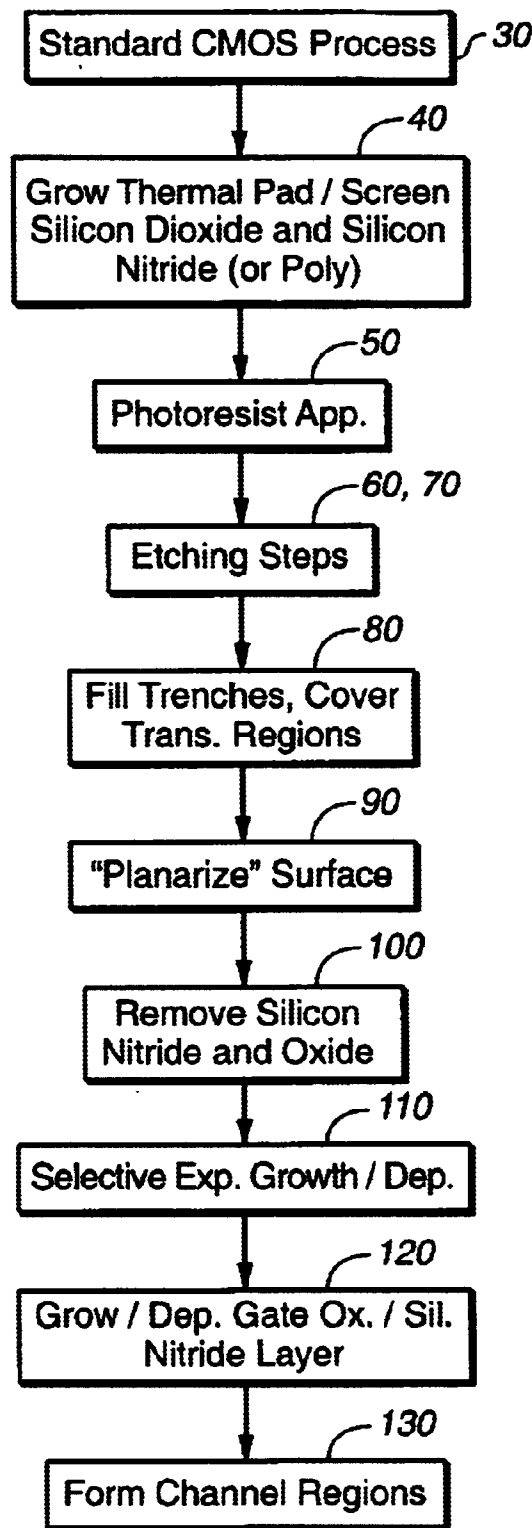
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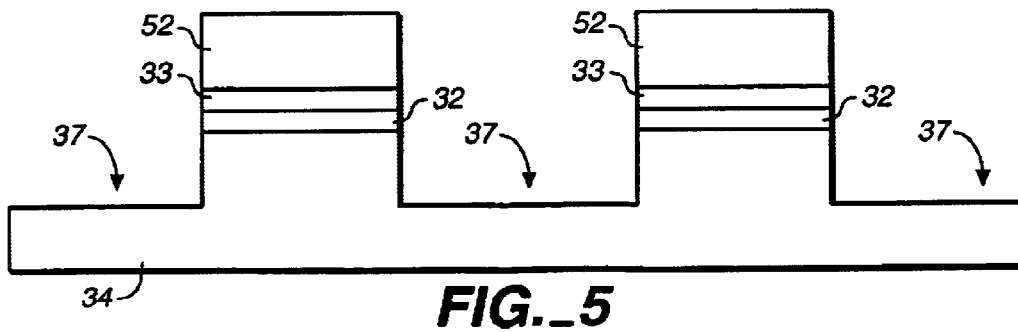
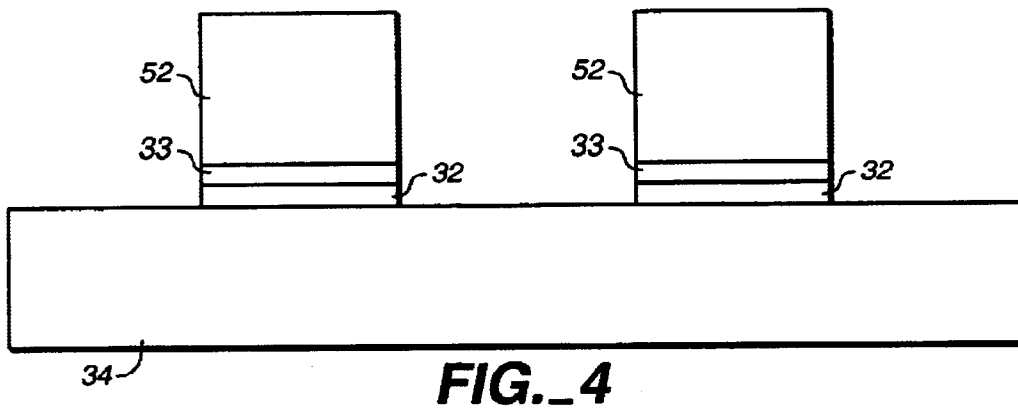
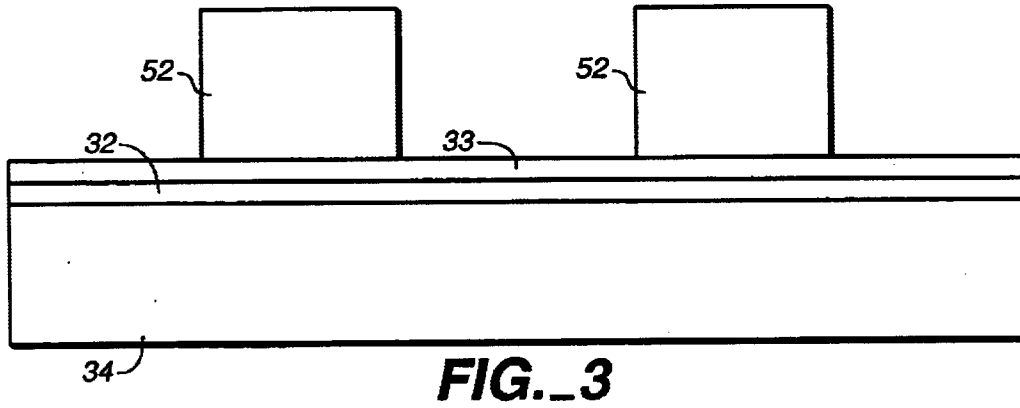
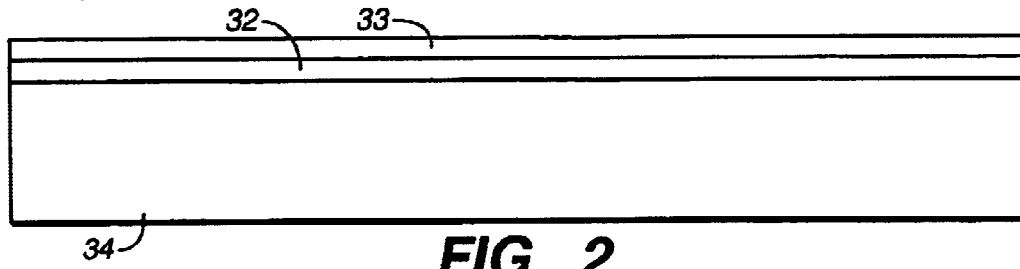
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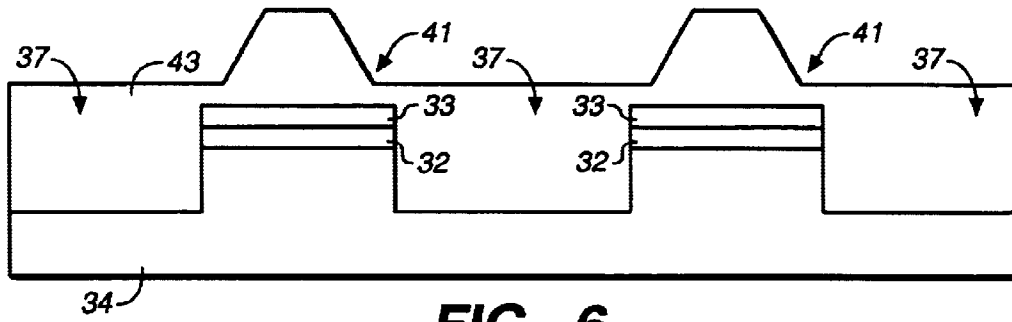
**18 Claims, 4 Drawing Sheets**



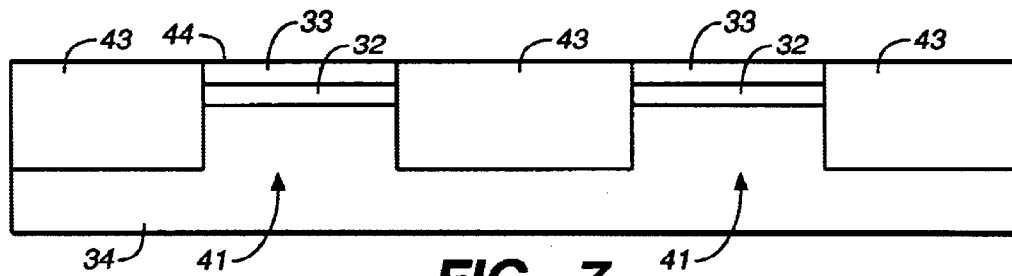


**FIG. 1**

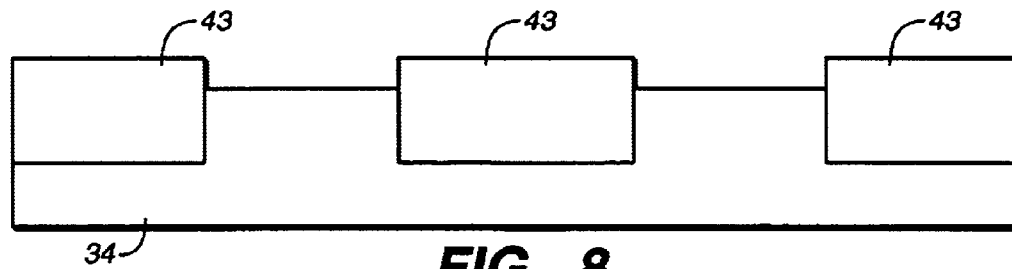




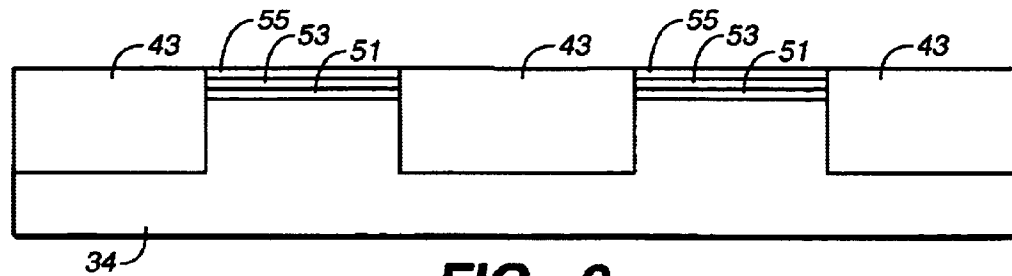
**FIG.\_6**



**FIG.\_7**



**FIG.\_8**



**FIG.\_9**

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