

EXHIBIT I

(12) **United States Patent**
Chen et al.

(10) **Patent No.:** **US 6,492,712 B1**
(45) **Date of Patent:** **Dec. 10, 2002**

(54) **HIGH QUALITY OXIDE FOR USE IN INTEGRATED CIRCUITS**
(75) Inventors: **Yuanning Chen**, Orlando, FL (US); **Sundar Srinivasan Chetlur**, Singapore (SG); **Sailesh Mansinh Merchant**, Orlando, FL (US); **Pradip Kumar Roy**, Orlando, FL (US)

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(73) Assignee: **Agere Systems Guardian Corp.**, Orlando, FL (US)

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

OTHER PUBLICATIONS

U.S. patent application Ser. No. 5,622,607, filed Nov. 15, 1991 and issued on Apr. 22, 1997 to Shunpei Yamazaki et al.

(21) Appl. No.: **09/597,077**

(22) Filed: **Jun. 20, 2000**

* cited by examiner

Related U.S. Application Data

(60) Provisional application No. 60/140,909, filed on Jun. 24, 1999.
(51) **Int. Cl.**⁷ **H01L 21/316**
(52) **U.S. Cl.** **257/632; 257/635**
(58) **Field of Search** **257/506, 524, 257/632, 635, 646**

Primary Examiner—Minh Loan Tran
Assistant Examiner—Thomas Dickey

(57) **ABSTRACT**

An oxide for use in integrated circuits is substantially stress-free both in the bulk and at the interface between the substrate and the oxide. The interface is planar and has a low interface trap density (N_{it}). The oxide has a low defect density and may have a thickness of less than 1.5 nm or less.

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15 Claims, 8 Drawing Sheets

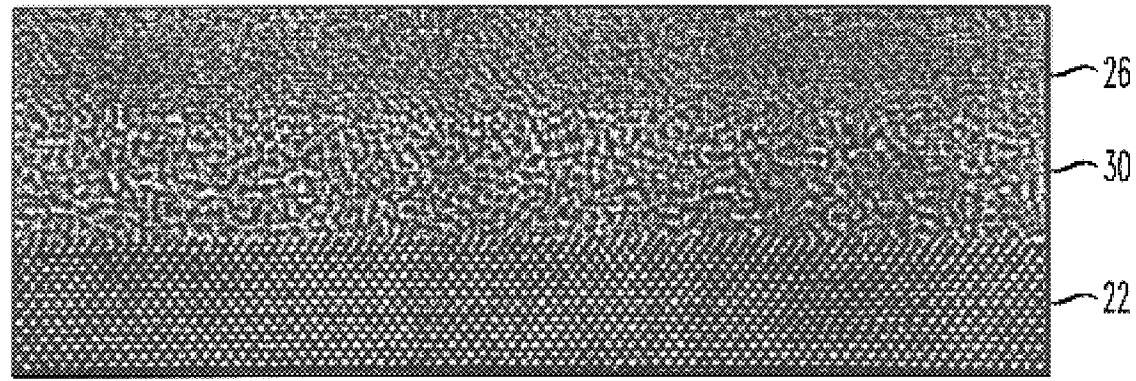


FIG. 1A

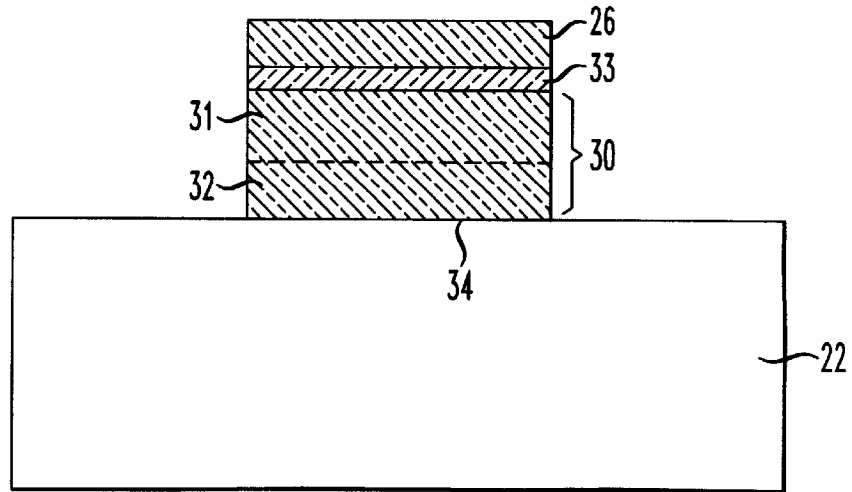


FIG. 1B

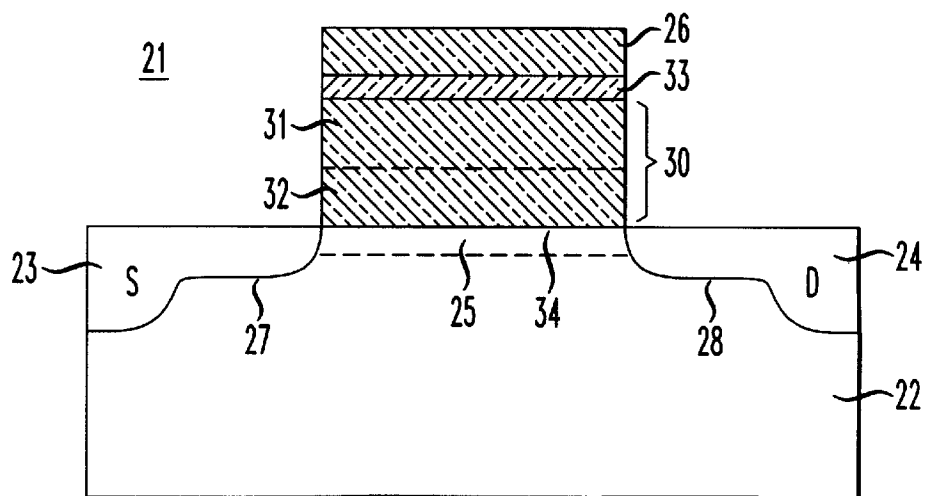


FIG. 2

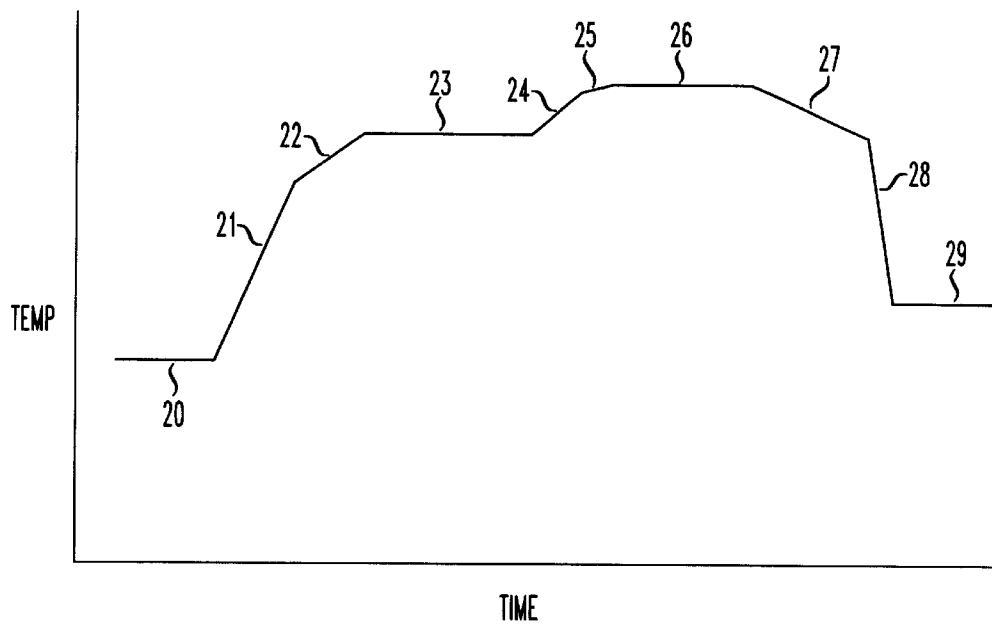


FIG. 3

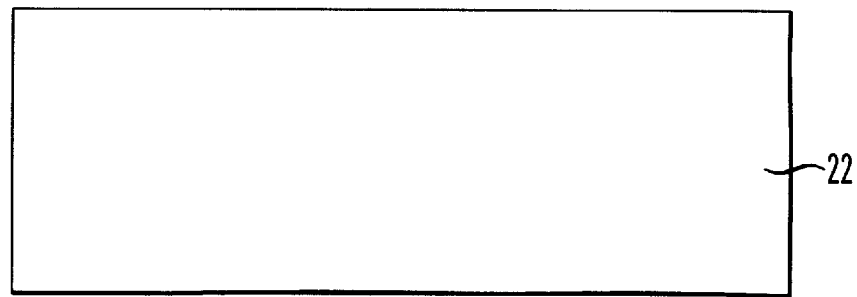


FIG. 4

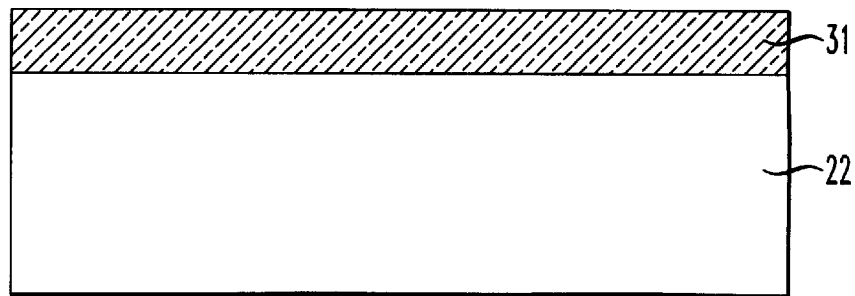
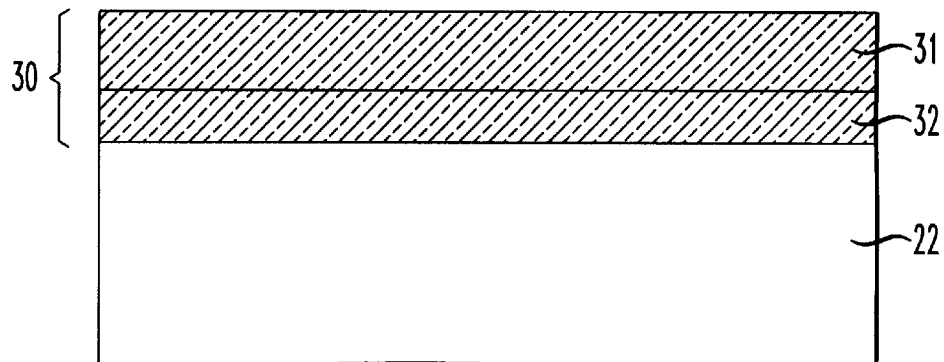


FIG. 5



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