

# EXHIBIT D

(12) **United States Patent**  
**Chou et al.**

(10) **Patent No.:** **US 6,177,843 B1**  
(45) **Date of Patent:** **Jan. 23, 2001**

(54) **OSCILLATOR CIRCUIT CONTROLLED BY PROGRAMMABLE LOGIC**

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(73) Assignee: **Cypress Semiconductor Corp.**, San Jose, CA (US)

(\*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **09/320,057**

(22) Filed: **May 26, 1999**

(51) Int. Cl.<sup>7</sup> ..... **H03L 7/08**; H03L 7/095

(52) U.S. Cl. .... **331/25**; 331/1 A; 331/16; 331/DIG. 2; 327/156; 327/159

(58) Field of Search ..... 331/1 A, 10, 11, 331/16, 17, 18, 25, DIG. 2; 327/2-12, 39-49, 156-159

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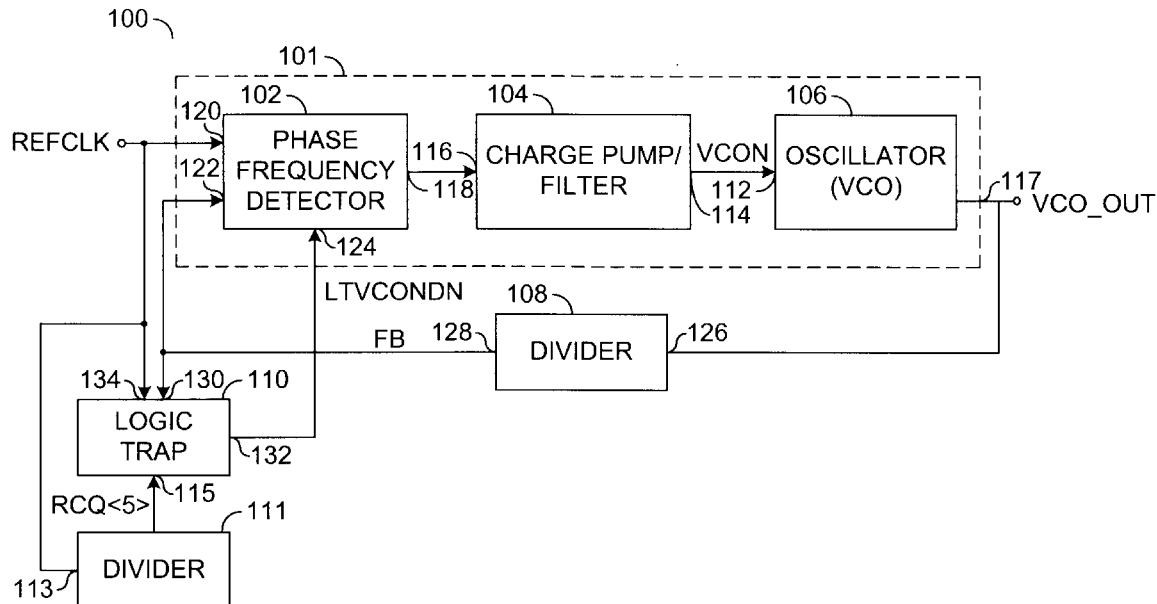
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(57) **ABSTRACT**

An apparatus comprising an oscillator circuit and a logic circuit. The oscillator circuit may be configured to present an output signal having a frequency in response to (i) a reference signal, (ii) a control signal and (iii) the output signal. The logic circuit may be configured to present the control signal in response to (i) the output signal and (ii) the reference signal. In one example, the logic circuit may disable the oscillator when the output signal oscillates outside a predetermined range.

**11 Claims, 6 Drawing Sheets**



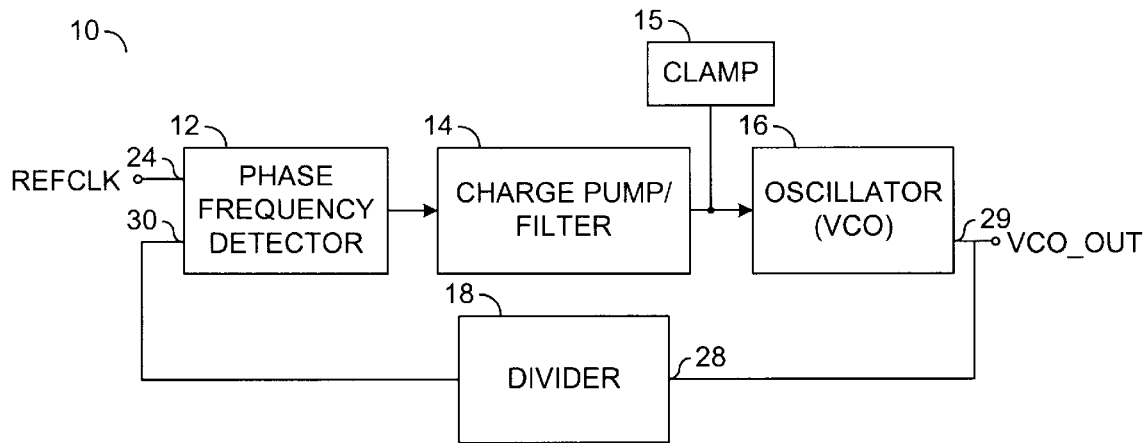


FIG. 1

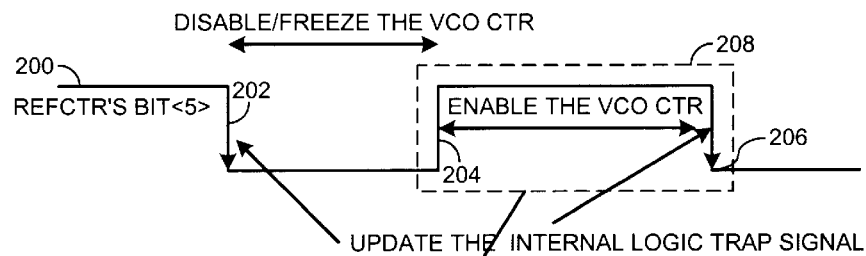


FIG. 5

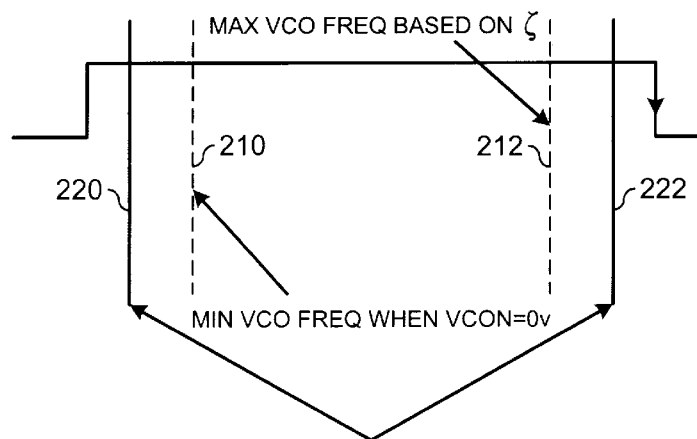
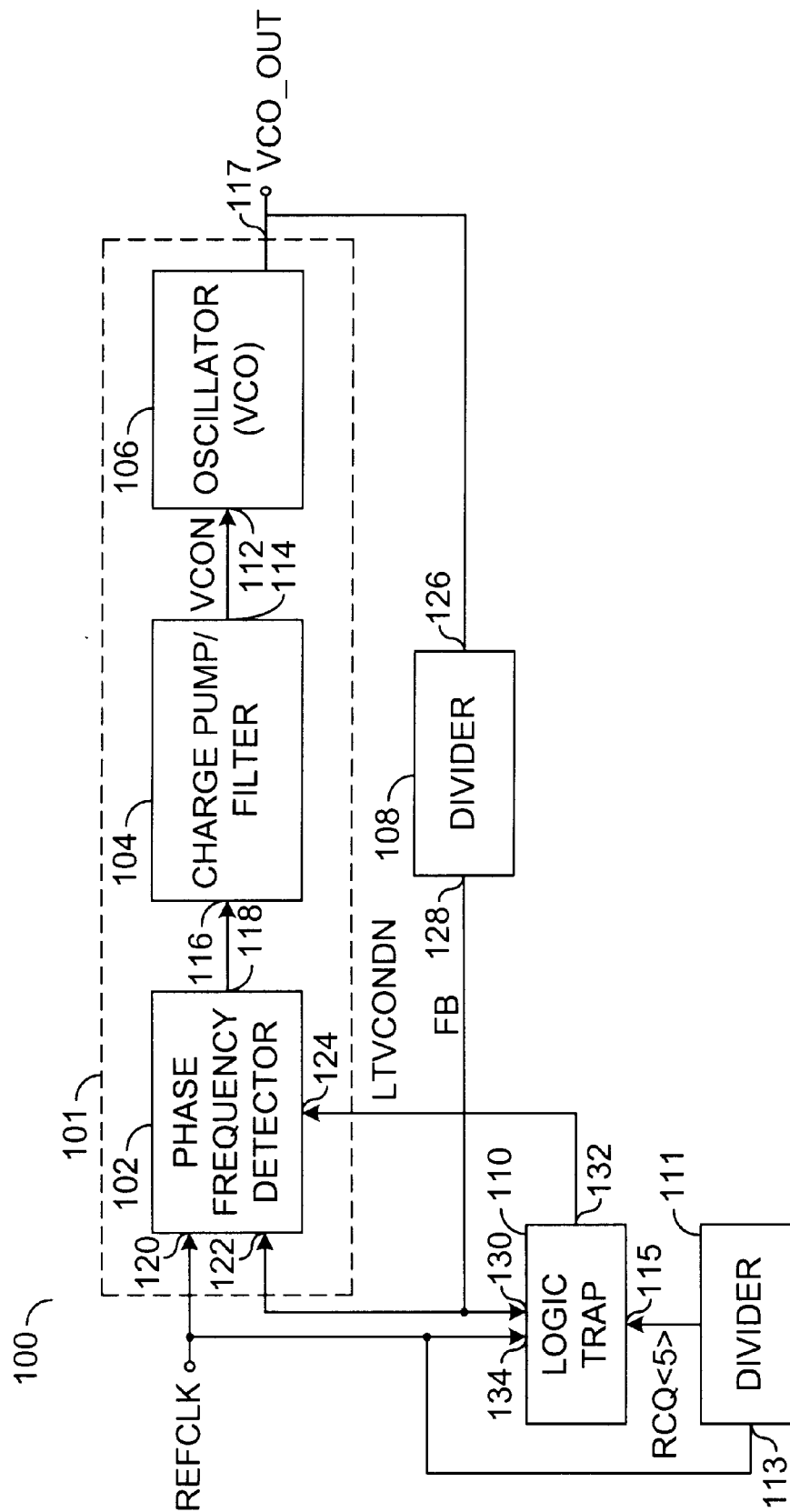


FIG. 6

LOGIC TRAPS MIN AND MAX PROGRAM THRESHOLDS

FIG. 2

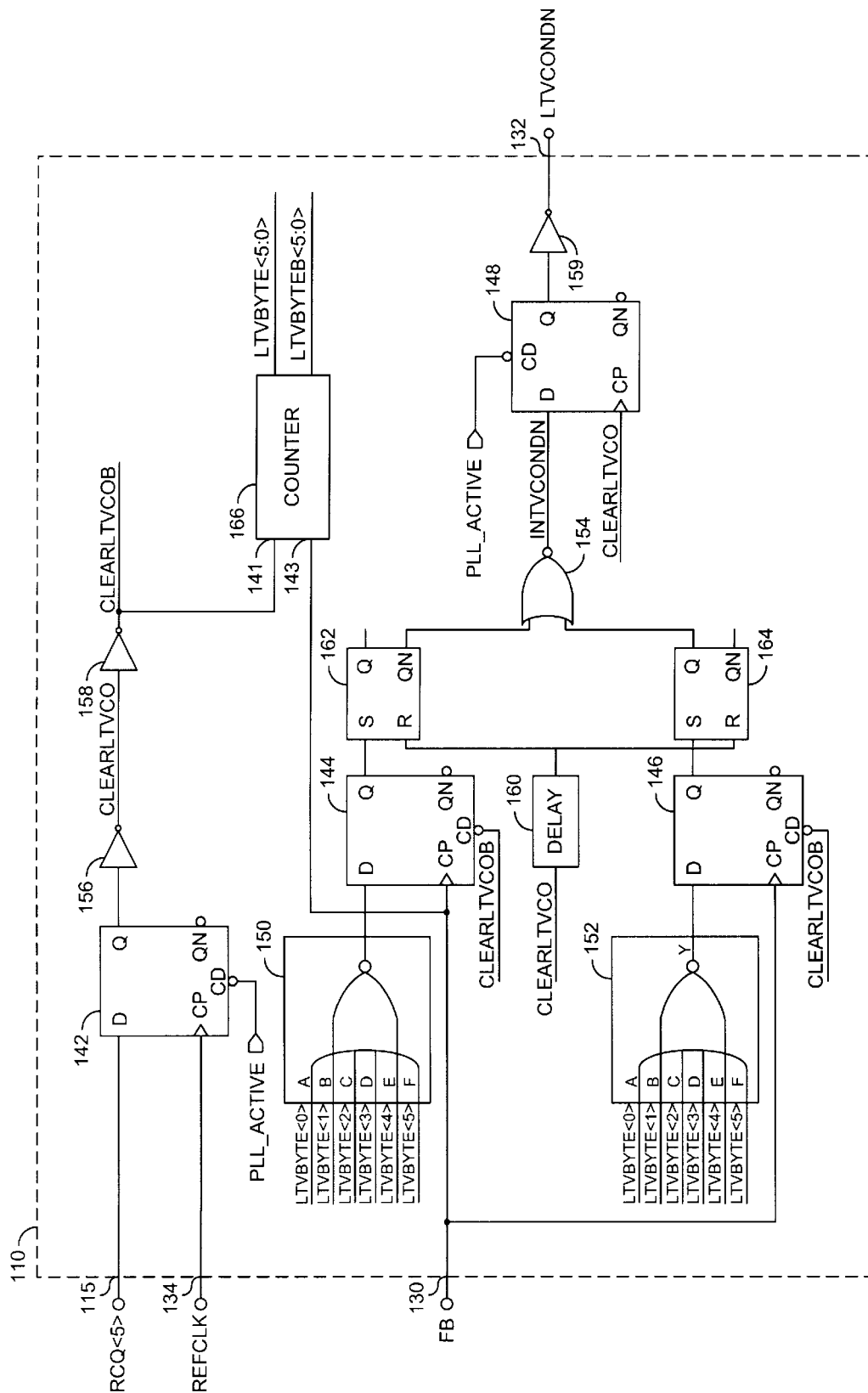


FIG. 3

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