EXHIBIT H

Analysis of Infringement of U.S. Patent No. 6,660,651 by Huawei Device USA Inc., Huawei Device Co., Ltd., and Ltd. (Based on Public Information Only)

Plaintiff Ocean Semiconductor LLC ("Ocean Semiconductor"), provides this preliminary and exemplary infringe infringement of U.S. Patent No. 6,660,651, entitled "ADJUSTABLE WAFER STAGE, AND A METHOD AND SYST PROCESS OPERATIONS USING SAME" (the "'651 patent") by Huawei Device USA Inc., Huawei Device Co., Ltd., Co., Ltd. ("Huawei"). The following chart illustrates an exemplary analysis regarding infringement by Defendant Huaw systems, devices, components, and integrated circuits, and products containing such circuits, fabricated or manufactured semiconductor fabrication or manufacturing equipment and/or platforms (e.g., ASML's TWINSCAN system). Such pro limitation, SoC chipsets and solutions (e.g., Hi3559A V100, Hi3519A V100, Hi3516D V300, Hi3556A V100, Hi3559 V Hi3559C V100, Hi3559 V100, Hi3716M V430, Hi3716M V430, Hi3798C V200, Hi3798M V200H, Hi3798M V300, H V200, Hi3798M V200, Hi3796M V100, Hi3798M V100, Hi3716M V420, Hi3716M V410, and Hi3751 V553), process Hi3536D V100, Hi3531D V100, Hi3521D V100, Hi3520D V400, Hi3520D V300, and Hi3520D V200), TV solutions (V101, Hi3751 V811, HI3751 V810, Hi3751 V551, Hi3751 V730, Hi3751 V620, Hi3751 V510, Hi3751 V310, Hi3751 V Kirin solutions (e.g., Kirin 9000/E, Kirin 1020, Kirin 990, Kirin 980, Kirin 970, Kirin 960, Kirin 950, Kirin 930, Kirin 9 710); Ascend solutions (e.g., Ascend 310 and Ascend 910); Kunpeng solutions (e.g., Kunpeng 920); and Balong solutio 5G01, Balong 765, Balong 750, Balong 720, Balong 710, and Balong 700), systems, products, or devices containing the systems, products, devices, and integrated circuits ("'651 Infringing Instrumentalities").

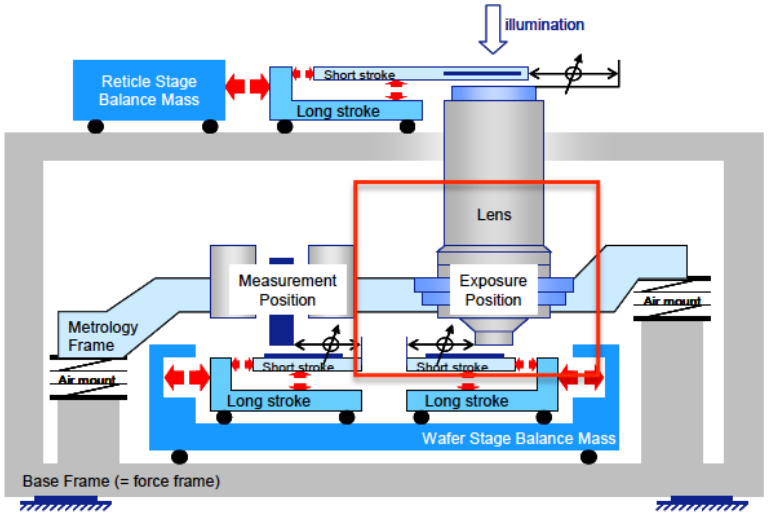
The analysis set forth below is based only upon information from publicly available resources regarding the '651 as Huawei has not yet provided any non-public information.

Unless otherwise noted, Ocean Semiconductor contends that Huawei directly infringes the '651 patent in violatio using, selling, and/or offering to sell in the United States, and/or importing into the United States, the '651 Infringing In following exemplary analysis demonstrates that infringement. Unless otherwise noted, Ocean Semiconductor further co below supports a finding of indirect infringement under 35 U.S.C. § 271(b) in conjunction with other evidence of liabilit

Unless otherwise noted, Ocean Semiconductor believes and contends that each element of each claim asserted he Huawei's provision or importation of the '651 Infringing Instrumentalities. However, to the extent that Huawei attempt claim element is not literally met, Ocean Semiconductor believes and contends that such elements are met under the doc specifically, in its investigation and analysis of the '651 Infringing Instrumentalities, Ocean Semiconductor did not iden differences between the elements of the patent claims and the corresponding features of the '651 Infringing Instrumental each instance, the identified feature of the '651 Infringing Instrumentalities performs at least substantially the same func way to achieve substantially the same result as the corresponding claim element.

Ocean Semiconductor notes that the present claim chart and analysis are necessarily preliminary in that Ocean Se
obtained substantial discovery from Huawei nor has Huawei disclosed any detailed analysis for its non-infringement pos
Semiconductor does not have the benefit of claim construction or expert discovery. Ocean Semiconductor reserves the r
amend the positions taken in this preliminary and exemplary infringement analysis, including with respect to literal infri
under the doctrine of equivalents, if and when warranted by further information obtained by Ocean Semiconductor, inclu
information adduced through information exchanges between the parties, fact discovery, claim construction, expert disc

USP No. 6,660,651	Infringement by the ’651 Accused Instrumentalities
19. A method, comprising: providing a process chamber comprised of a wafer stage, said wafer stage having a surface that is adjustable;	ASML’s TWINSCAN system provides a process chamber comprised of a wafer stage, t surface that is adjustable. For example, the TWINSCAN system performs the method of providing a process chan  *See* ASML DUV Lithography Systems, *available at* https://www.asml.com/en/products systems/twinscan-nxt1980di (last visited Apr. 30 2019). The process chamber can be used for wafer exposure during lithography:

	 *Figure 5. TWINSCAN^{TM} dynamic architecture* *See* Perspective on Stage Dynamics and Control at 3. The process chamber includes an adjustable wafer stage having a surface that is adjustal "In Figure 4, the table holding the wafer is called the mirror block because of the mirror allow interferometric position measurement (IFM)." *See* Position Control at 31. For example, the adjustable wafer stage or mirror block of the TWINSCAN system is sl

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