EXHIBIT 5

U.S. Patent No. 9,858,218

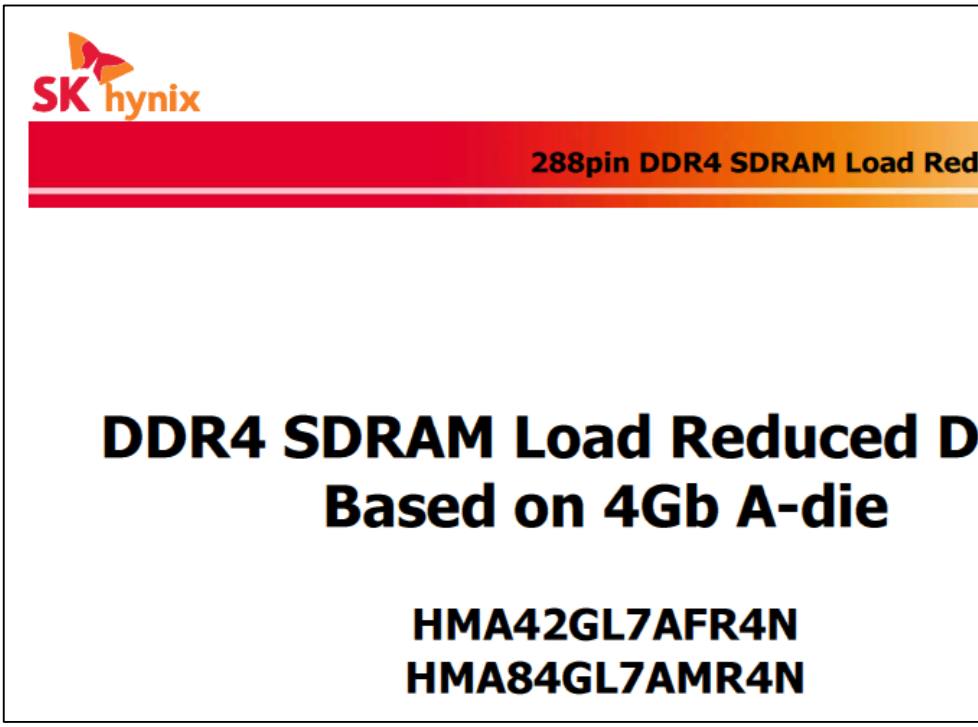
SK hynix HMA84GL7AMR4N-UHTE

U.S. Patent No. 9,858,218: Claim 1

"1. A memory module operable with a memory controller of a host system, comprising:"

1. A memory module operable with a memory controller of a host system, comprising:	The SK hynix Products are memory modules operable with a memory controller of a host sys For example, the SK hynix Products are DDR4 load reduced dual in-line memory modules (“

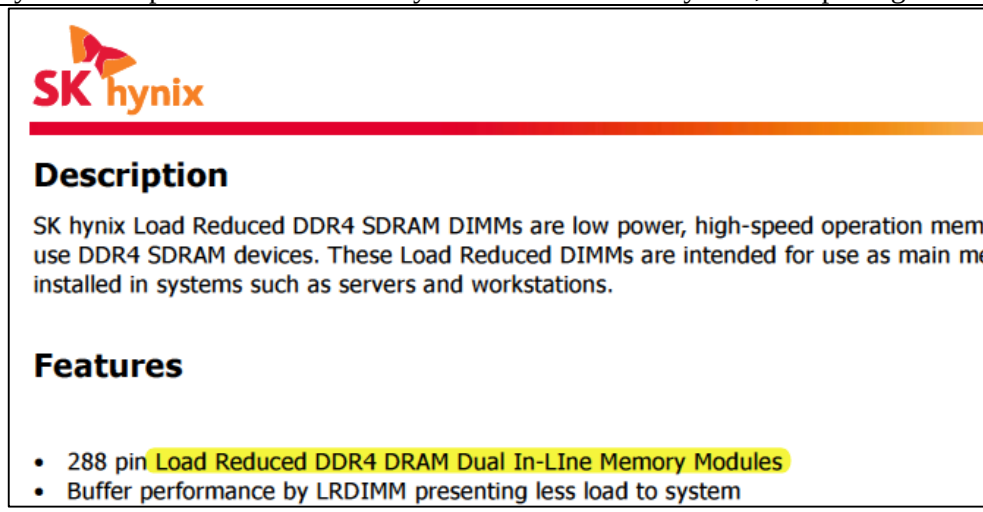
(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).



SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet, at 1.

U.S. Patent No. 9,858,218: Claim 1

"1. A memory module operable with a memory controller of a host system, comprising:"



SK hynix

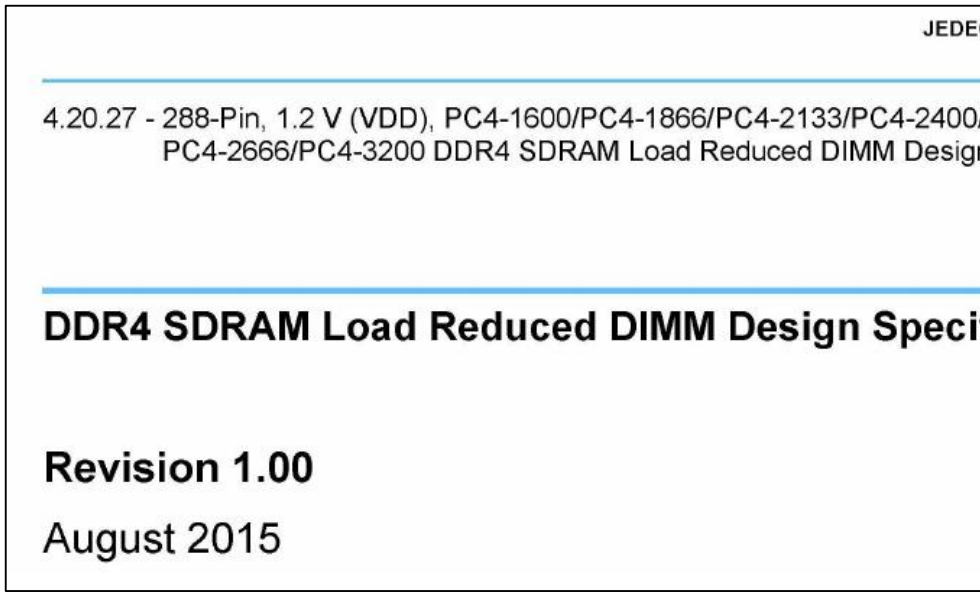
Description

SK hynix Load Reduced DDR4 SDRAM DIMMs are low power, high-speed operation mem
use DDR4 SDRAM devices. These Load Reduced DIMMs are intended for use as main me
installed in systems such as servers and workstations.

Features

- 288 pin Load Reduced DDR4 DRAM Dual In-LIne Memory Modules
- Buffer performance by LRDIMM presenting less load to system

SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 3 (annotation added).



JEDE

4.20.27 - 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/
PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Desig

DDR4 SDRAM Load Reduced DIMM Design Speci

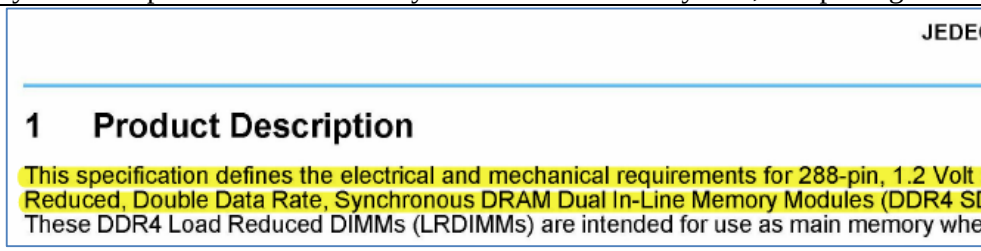
Revision 1.00

August 2015

JEDEC LRDIMM Specification at 1.

U.S. Patent No. 9,858,218: Claim 1

"1. A memory module operable with a memory controller of a host system, comprising:"



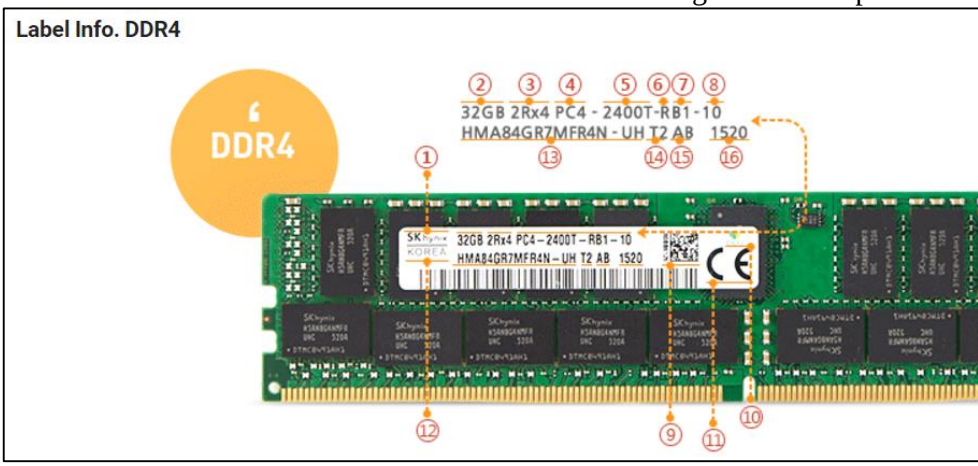
JEDE

1 Product Description

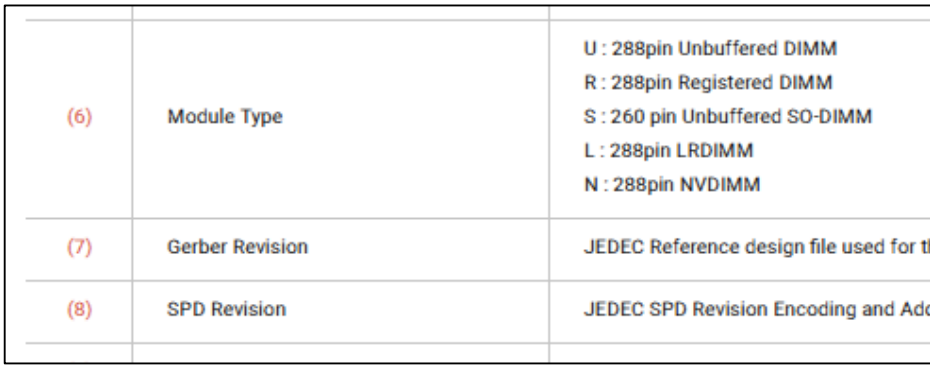
This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt
Reduced, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SD
These DDR4 Load Reduced DIMMs (LRDIMMs) are intended for use as main memory whe

JEDEC LRDIMM Specification at 5 (annotation added).

The SK hynix HMA84GL7AMR4N-UHTE is manufactured according to JEDEC specificatio



See SKH DDR4 Module Label Info at 3.



(6)	Module Type	U : 288pin Unbuffered DIMM R : 288pin Registered DIMM S : 260 pin Unbuffered SO-DIMM L : 288pin LRDIMM N : 288pin NVDIMM
(7)	Gerber Revision	JEDEC Reference design file used for t
(8)	SPD Revision	JEDEC SPD Revision Encoding and Ado

See SKH DDR4 Module Label Info at 3.

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