

Exhibit 1

(12) **United States Patent**
Levy et al.

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(54) **CONCURRENT SERIAL INTERCONNECT FOR INTEGRATING FUNCTIONAL BLOCKS IN AN INTEGRATED CIRCUIT DEVICE**

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(73) Assignee: **Philips Semiconductors Inc., New York, NY (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/201,450**

(22) Filed: **Nov. 30, 1998**

(51) **Int. Cl.**⁷ **G06F 13/00; G06F 13/14**

(52) **U.S. Cl.** **710/129; 710/126**

(58) **Field of Search** **710/129-132, 710/38; 709/252-253; 370/360-385, 498-545**

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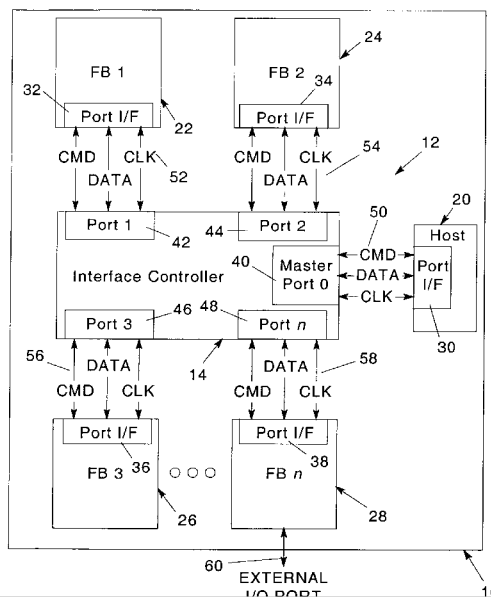
Primary Examiner—Sumati Lefkowitz

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(57) **ABSTRACT**

A circuit arrangement and method interface multiple functional blocks within an integrated circuit device via a concurrent serial interconnect capable of routing separate serial command, data and clock signals between functional blocks in the device. The concurrent serial interconnect utilizes a plurality of serial ports that are selectively coupled to one another by an interface controller to define one or more logical communication channels between two or more of the serial ports. Each serial port is coupled via a point-to-point interconnection with a port interface in a functional block. In addition, the concurrent serial interconnect facilitates the design of an integrated circuit device by supporting the addition of a serial interconnect to an assemblage of functional blocks, with each functional block associated with one of a plurality of serial ports in the serial interconnect.

40 Claims, 9 Drawing Sheets



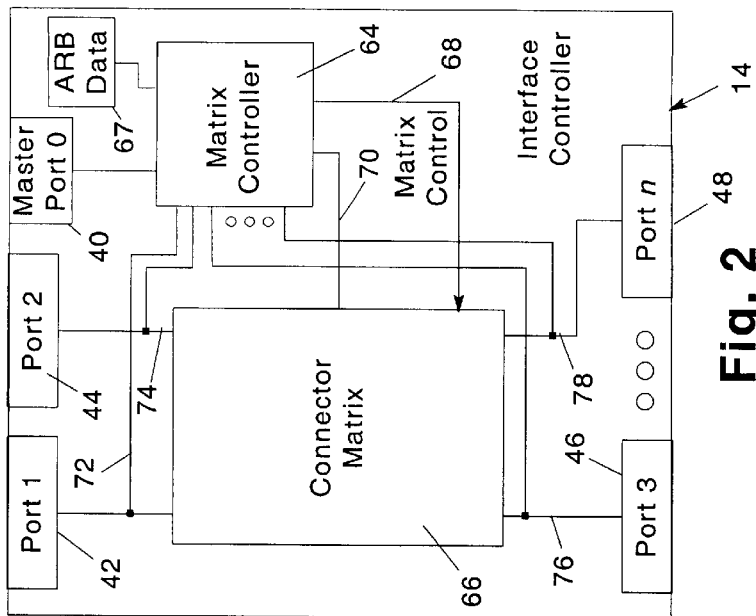


Fig. 2

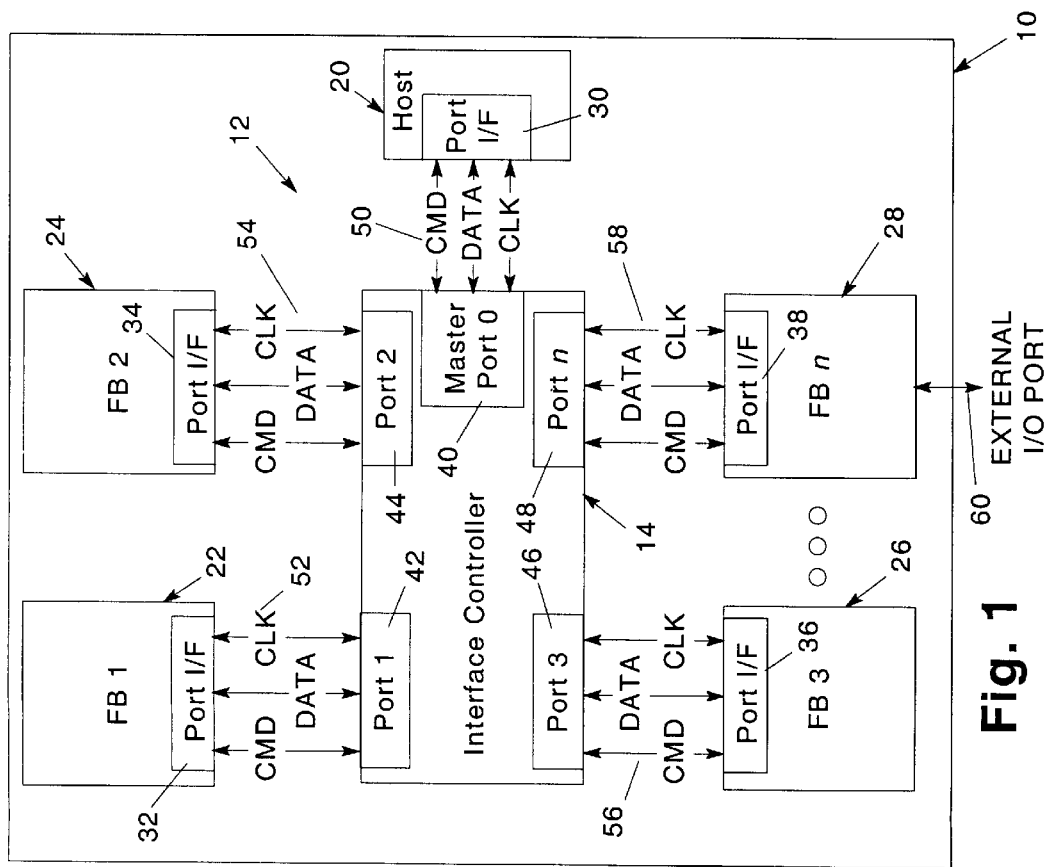


Fig. 1

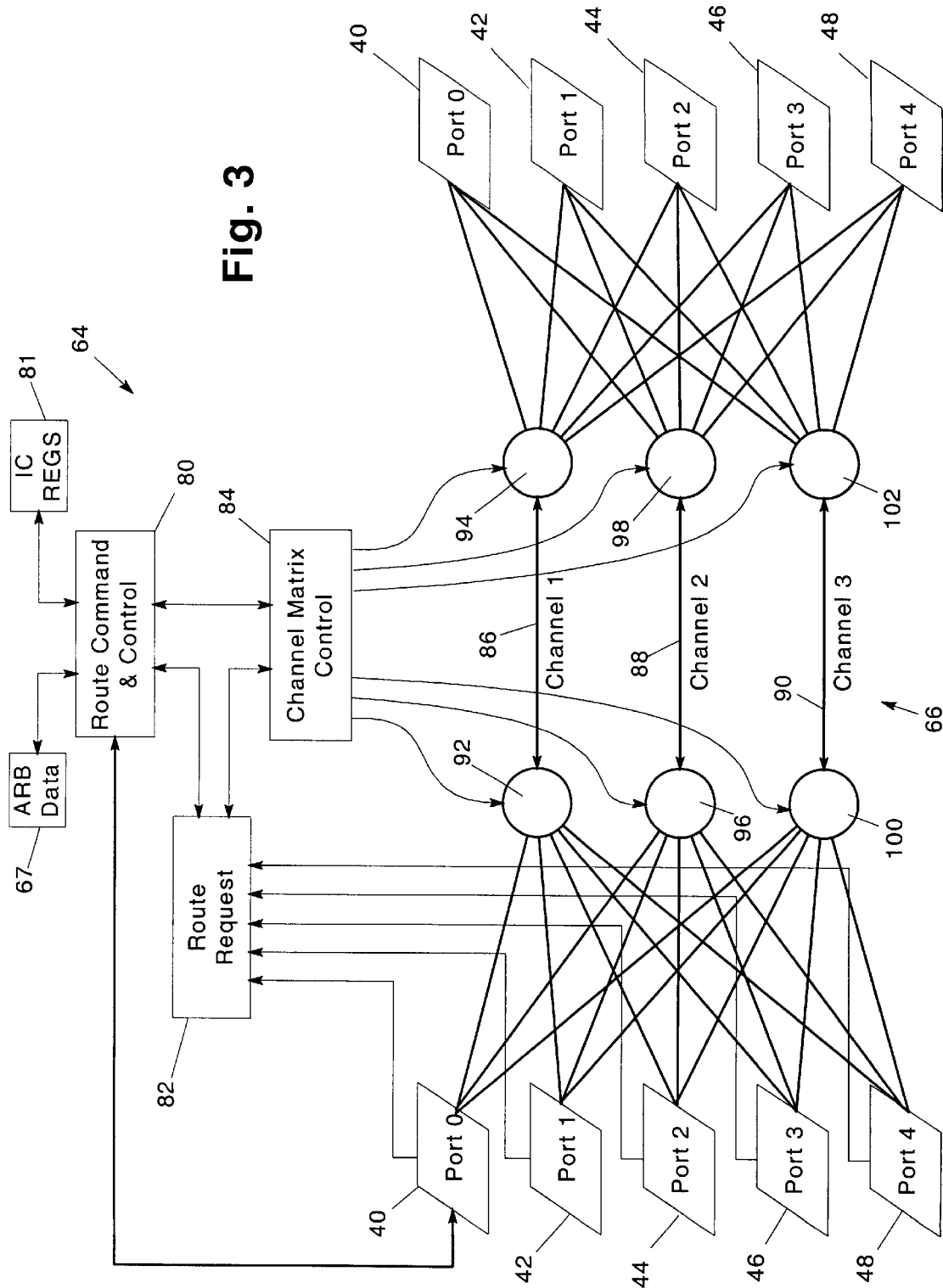
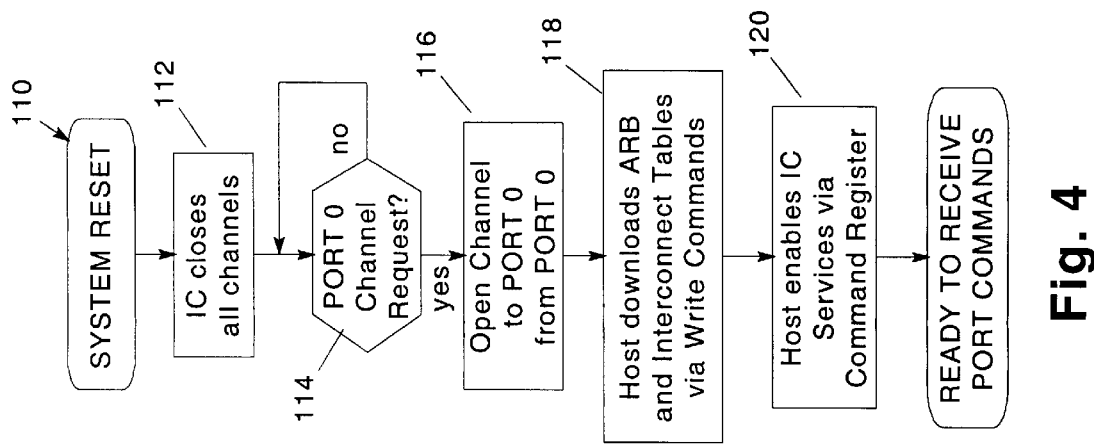
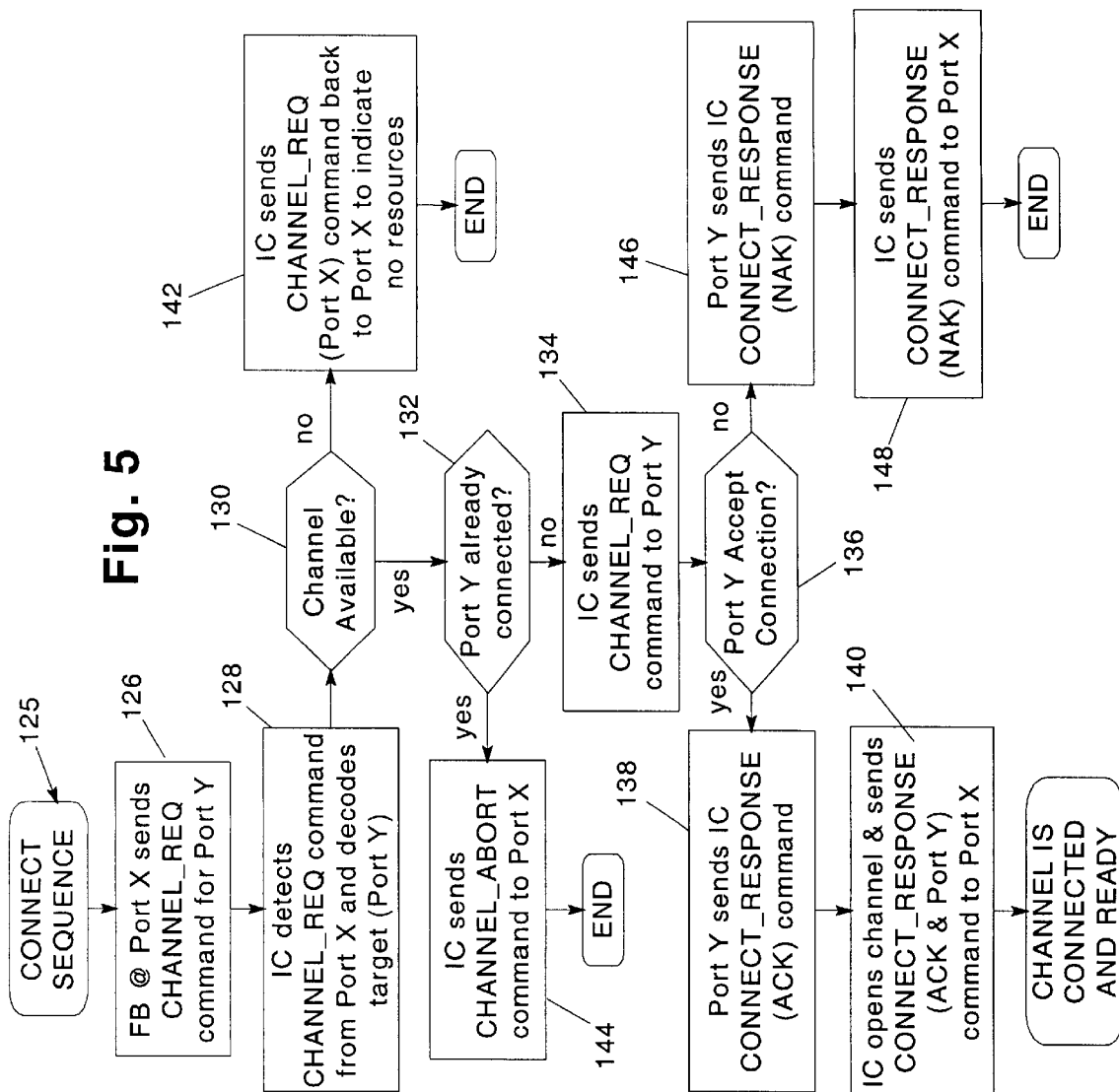


Fig. 3



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