United States Court of Appeals for the Federal Circuit

POLARIS INNOVATIONS LIMITED,
Appellant

v.

DERRICK BRENT, DEPUTY UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DEPUTY DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Intervenor

2019-1483

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-01500.

POLARIS INNOVATIONS LIMITED,
Appellant

v.

DERRICK BRENT, DEPUTY UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DEPUTY DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Intervenor

2019-1484

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-00901.

Decided: September 15, 2022

MATTHEW C. PHILLIPS, Laurence & Phillips IP Law LLP, Washington, DC, argued for appellant. Also represented by KEVIN BRENT LAURENCE, DEREK MEEKER; PAUL EHRLICH, MATTHEW D. POWERS, STEFANI SMITH, Tensegrity Law Group LLP, Redwood Shores, CA.

MAUREEN DONOVAN QUELER, Office of the Solicitor, United States Patent and Trademark Office, Alexandria, VA, argued for intervenor in 2019-1483. Also argued by OMAR FAROOQ AMIN in 2019-1484. Also represented by THOMAS W. KRAUSE, ROBERT J. MCMANUS, FARHEENA YASMEEN RASHEED; MICHAEL S. FORMAN in 2019-1483; MELISSA N. PATTERSON, Appellate Staff, Civil Division, United States Department of Justice, Washington, DC.

Before PROST, CHEN, and STOLL, *Circuit Judges*.

STOLL, *Circuit Judge*.

These appeals involve two inter partes review proceedings initiated by NVIDIA Corporation challenging two patents owned by Polaris Innovations Limited—U.S. Patent Nos. 6,532,505 and 7,405,993. The Patent Trial and Appeal Board determined that all challenged claims are unpatentable. Polaris appealed. We remanded the case due

to Appointments Clause issues and it has now returned. We affirm.

BACKGROUND

I

These appeals involve two unrelated patents directed to computer memory. The '993 patent, at issue in the 19-1484 appeal, relates to an improved control component configuration. The '505 patent, at issue in the 19-1483 appeal, involves a shared-resource system in which logical controls are used to manage resource requests.

A

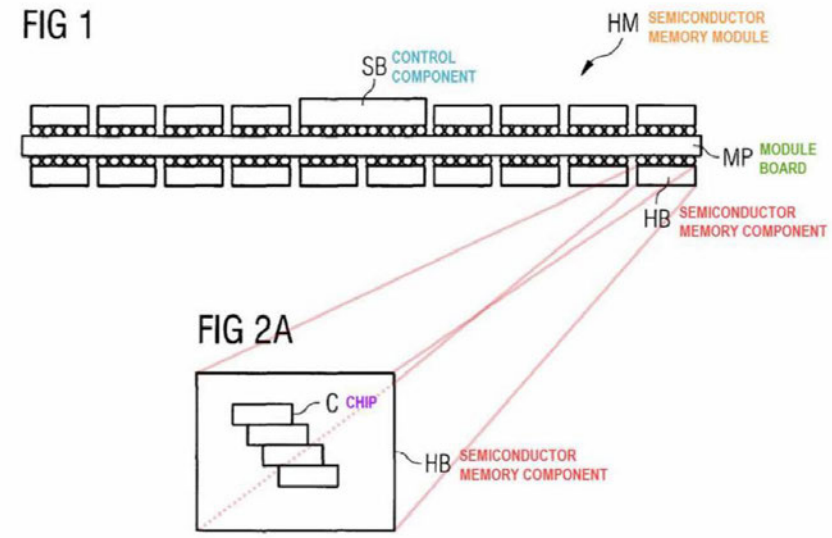
The '993 patent is titled "Control Component for Controlling a Semiconductor Memory Component in a Semiconductor Memory Module." '993 patent, Title. The specification explains that the control component can send both address signals and control signals through the same leads, allowing the control component to perform its functions with fewer leads. *See, e.g.*, *id.* at col. 2 l. 57–col. 3 l. 23.

On appeal, Polaris's argument focuses on dependent claim 2's requirement that the "semiconductor memory component comprises a plurality of memory chips." *Id.* at col. 11 ll. 39–40. Claim 2 (and independent claim 1 from which claim 2 depends) recites:

> 1. A control component for controlling a semiconductor memory component in a semiconductor memory module, comprising:
>
> a control unit for generating control signals for controlling read and write access to the semiconductor memory component and for generating address signals for addressing memory cells in the semiconductor memory component for read and write access;

> a plurality of address terminals for providing the address signals; and
>
> a selection circuit for supplying one of the address terminals with a selected signal selected between one of the address signals and one of the control signals.
>
> 2. The control component as claimed in claim 1,
>
> *wherein the semiconductor memory component comprises a plurality of memory chips*; and
>
> wherein the control unit generates a first of the control signal for selecting one of the memory chips for read and write access.

Id. at col. 11 ll. 25–43 (emphasis added to disputed limitation). Polaris correlates the terms in claim 2 to Figures 1 and 2 of the '993 patent, shown in a combined fashion below:



19-1484 Appellant's Br. 7 (annotating '993 patent, Figs. 1 & 2A). As described in the claims and shown in the figures above, the chips (C) are a part of the semiconductor memory component (HB) which is integrated into the

semiconductor memory module (HM). The semiconductor memory module also includes a control component (SB).

B

The '505 patent describes a "universal resource access controller" (104) for directing requests for a shared resource, such as a shared memory (108):

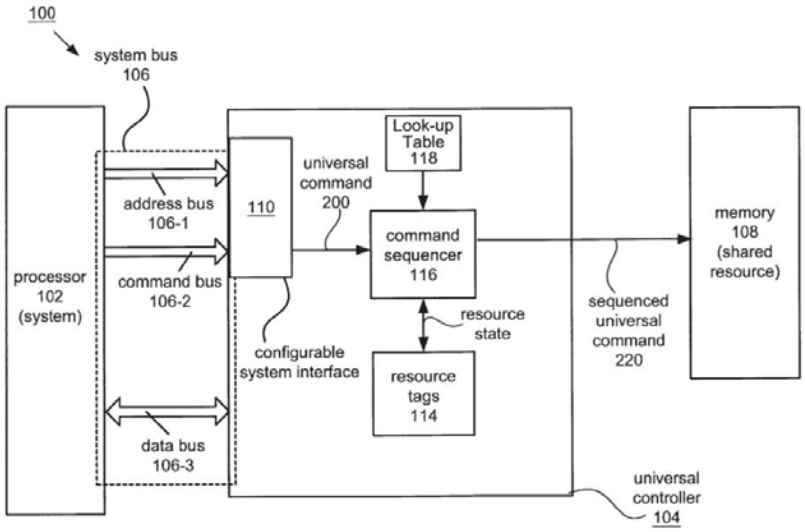


Fig. 1B

'505 patent, Fig. 1B; *see also id.* at Title.

The '505 patent discloses that the controller uses certain information to direct shared-resource requests, including: (1) the "current state" of the shared resource, *id.* at col. 7 ll. 3–29, (2) the "requested state" of a shared resource, *id.* at col. 27 l. 41–col. 30 l. 19, and (3) a "characteristic operating parameter" of the shared resource, *id.* at col. 7 l. 61–col. 8 l. 23, col. 8 l. 56–col. 9 l. 5. The dispute on appeal centers on this shared-resource request information, and in particular where that information is stored. Dependent claim 2 requires these pieces of information to be stored in certain "buffers," as recited below:

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