United States Court of Appeals for the Federal Circuit

VLSI TECHNOLOGY LLC,
Appellant

v.

INTEL CORPORATION,
Appellee

2021-1826, 2021-1827, 2021-1828

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2019-01198, IPR2019-01199, IPR2019-01200.

Decided: November 15, 2022

NATHAN NOBU LOWENSTEIN, Lowenstein & Weatherwax LLP, Santa Monica, CA, argued for appellant. Also represented by KENNETH J. WEATHERWAX.

S. CALVIN WALDEN, Wilmer Cutler Pickering Hale and Dorr LLP, New York, NY, argued for appellee. Also represented by JEFFREY ANDREW DENNHARDT; MARK CHRISTOPHER FLEMING, JOHN V. HOBGOOD, STEPHANIE LIN, Boston, MA; RONALD GREGORY ISRAELSEN, Washington, DC.

Before CHEN, BRYSON, and HUGHES, *Circuit Judges*.

BRYSON, *Circuit Judge*.

Appellee Intel Corporation filed three petitions for *inter partes* review ("IPR") of U.S. Patent No. 7,247,552 ("the '552 patent"), which is owned by appellant VLSI Technology LLC. The Patent Trial and Appeal Board instituted the IPR proceedings, and in a combined Final Written Decision, the Board found all of the challenged claims of the '552 patent to be unpatentable. For the reasons set forth below, we affirm in part, reverse in part, and remand.

I

A

The '552 patent is directed to "[a] technique for alleviating the problems of defects caused by stress applied to bond pads" of an integrated circuit. '552 patent, Abstract.

An integrated circuit, sometimes referred to as a "chip" or "die," contains numerous electronic circuits that are integrated on a flat piece of semiconductor called a "substrate." The specification of the '552 patent discloses an integrated circuit that includes several metal "interconnect layers" positioned above the substrate and frequently surrounded by "dielectric" or insulating material. *See id.* at col. 3, ll. 1–10 & Fig. 1. The integrated circuits described in the '552 patent also include one or more "bond pads" that sit above the interconnect layers and are used to attach the chip to another electronic component, such as a computer motherboard. *See id.* at col. 3, ll. 22–25.

When a chip is attached to another electronic component, forces are exerted on the chip's bond pad. *Id.* at Abstract & col. 5, ll. 53–57. Those forces can result in damage to the interconnect layers and to the dielectric material that surrounds those layers. *See id.* at Abstract & col. 1, ll. 39–42. As such, dedicated support structures made of metal layers and vias are connected to and provide support

for the bond pad. *See id.* at col. 1, ll. 53–61. In the prior art, these metal support layers were linked to the bond pad, and thus were not "functionally independent," i.e., they could not be "used for wiring or interconnects unrelated to the pad." *Id.* at col. 1, ll. 58–64.

The '552 patent discloses improvements to the structures of an integrated circuit that reduce the potential for damage to the interconnect layers and dielectric material when the chip is attached to another electronic component while also "permit[ing] each of the interconnect layers underlying [the pad] to be functionally independent in the circuit if desired." *See id.* at col. 3, line 64 through col. 4, line 7. Specifically, the '552 patent discloses that only "a predetermined minimum amount of metal or a minimum density" is needed to "adequately support" the bond pad. *See id.* at col. 3, line 64 through col. 4, line 4. If the functionally independent interconnect layers underneath the pad are insufficient to reach a predetermined minimum density, "dummy metal lines"—i.e., metal lines that do not serve any electrical purpose—may be added to increase the metal density of the interconnect layers. *See id.* at col. 4, ll. 13–56; *see also id.* at Fig. 3.

Claim 1 is the only independent apparatus claim of the '552 patent and is representative of the claimed invention. It recites as follows:

> 1. An integrated circuit, comprising:
>
> a substrate having active circuitry;
>
> a bond pad over the substrate;
>
> a force region at least under the bond pad characterized by being susceptible to defects due to stress applied to the bond pad;
>
> a stack of interconnect layers, wherein each interconnect layer has a portion in the force region; and

> a plurality of interlayer dielectrics separating the interconnect layers of the stack of interconnect layers and having at least one via for interconnecting two of the interconnect layers of the stack of interconnect layers;
>
> wherein at least one interconnect layer of the stack of interconnect layers comprises a functional metal line underlying the bond pad that is not electrically connected to the bond pad and is used for wiring or interconnect to the active circuitry, the at least one interconnect layer of the stack of interconnect layers further comprising dummy metal lines in the portion that is in the force region to obtain a predetermined metal density in the portion that is in the force region.

'552 patent, claim 1. Claim 2 depends from claim 1, and claim 11 is a method claim generally similar to claim 1.

Claim 20 also plays a role in this appeal. It recites as follows:

> 20. A method of making an integrated circuit having a plurality of bond pads, comprising:
>
> developing a circuit design of the integrated circuit;
>
> developing a layout of the integrated circuit according to the circuit design, wherein the layout comprises a plurality of metal-containing interconnect layers that extend under a first bond pad of the plurality of bond pads, at least a portion of the plurality of metal-containing interconnect layers underlying the first bond pad and not electrically connected to the bond pad as a result of being used for electrical interconnection not directly connected to the bond pad;

> modifying the layout by adding dummy metal lines to the plurality of metal-containing interconnect layers to achieve a metal density of at least forty percent for each of the plurality of metal-containing interconnect layers; and
>
> forming the integrated circuit comprising the dummy metal lines.

'552 patent, claim 20.

B

In 2018, VLSI brought suit in the United States District Court for the District of Delaware, charging Intel with infringing the '552 patent. The district court subsequently conducted a claim construction hearing. In the course of the hearing, the court construed the term "force region," which appears in independent claims 1 and 11 of the '552 patent. Citing a passage from the '552 patent, the district court construed "force region" to mean a "region within the integrated circuit in which forces are exerted on the interconnect structure when a die attach is performed." J.A. 6017, 6356; *see also* '552 patent, col. 3, ll. 49–52.

In June 2019, after the district court action was filed but before the claim construction proceedings in that action, Intel filed its petitions for IPR, challenging the validity of claims 1, 2, 11, and 20 of the '552 patent. In the petition directed to claims 1 and 2, Intel proposed a construction of "force region" that was consistent with the claim construction that Intel subsequently offered to the district court and that the district court adopted, i.e., a "region within the integrated circuit in which forces are exerted on the interconnect structure when a die attach is performed." J.A. 6588–89.

VLSI did not oppose Intel's proposed construction before the Board. It soon became evident, however, that although the parties purported to agree on the construction to be given to the term "force region," their agreement was

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