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17/987,828	11/15/2022	Danillo Graziosi	SONY-75200	6471
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Specification

2. The disclosure is objected to because of the following informalities:
 - In page 3, lines 4-5, "from the pixels' surfaces" should read "from the surface's pixels".
 - In page 5, line 13, "from the pixels' surfaces" should read "from the surface's pixels".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis (i.e., changing from AIA to pre-AIA) for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.
4. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-2, 4-7, 8-9, and 12-14 are rejected under 35 U.S.C. 103 as being unpatentable over Graziosi et al. ([V-PCC] [specification] Depth range adjustment, ISO/IEC JTC 1/SC 29/WG 11 m51170, Geneva, CH, October 2019, hereinafter "Graziosi_VPCC"), and in view of:

- Schwalb et al. (Fast Motion Estimation on Graphics Hardware for H.264 Video Encoding IEEE Transactions on Multimedia (Volume: 11, Issue: 1, 2009, Page(s): 1-10), hereinafter "Schwalb")
- Wei et al. (Bi-Normal Filtering for Mesh Denoising, IEEE Transactions on Visualization and Computer, Vol. 21, No. 1, January 2015, hereinafter "Wei").
- Nakagawa et al. (Estimating Surface Normals with Depth Image Gradients for Fast and Accurate Registration, 2015 International Conference on 3D Vision (2015, Page(s): 640-647), hereinafter "Nakagawa")

Regarding claim 1, Graziosi_VPCC teaches A method of mesh geometry coding comprising: (section 1, "the luminance values carry the depth value")

mapping depth information to a luma channel using fewer than all available bits; (section 1, "the luminance values carry the depth value. The decoded bit depth is adjusted according to the 2D nominal bit depth value (indicated by the syntax element `gi~geometry_nominaf_2d_bitdepth_minusl`). The adjustment will either only clip the values ... or scale them by a power of two"). Note that the luma channel with the

luminance values contains depth information, and the “clipping” or “scaling” indicates that the least significant bits or most significant bits are ignored/unused.

generating a depth scaling factor which is incorporated into a bilinear interpolation algorithm used during rasterization; and (section 1, “The decoded bit depth is adjusted according to the 2D nominal bit depth value ... scale them by a power of two (in case the MSBs are to be aligned)”).

However, Graziosi_VPCC does not disclose **incorporated into a bilinear interpolation algorithm used during rasterization.**

In the same art of video coding, Schwalb discloses **incorporated into a bilinear interpolation algorithm used during rasterization** (Schwalb, page 3, section 3, “to generate so called “fragments” for all output pixels that the currently rendered triangle covers. A fragment is a data structure analog to the structure of a vertex and is calculated by the Rasterizer by interpolating position coordinates”; page 5, section 4, “Supersampling to a factor of 4 with bilinear interpolation”). Note that during rasterization the bilinear interpolation gets the scaling factor involved for calculations to have the depth values scaled to the bit-depth.

Graziosi_VPCC and Schwalb are in the same field of endeavor, namely computer graphics. Before the effective filing date of the claimed invention, it would have been obvious to apply the bilinear interpolation during rasterization, as taught by Schwalb into Graziosi_VPCC. The motivation would have been “calculated by the Rasterizer by interpolating position coordinates” (Schwalb, page 3, section 3). The suggestion for doing so would allow to perform rasterization with a bilinear interpolation

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